CHARACTERIZATION OF GAN TRANSISTORS AND DEVELOPMENT OF BI-DIRECTIONAL DC/DC CONVERTER WITH HALF-BRIDGE HAVING SHORT CIRCUIT PROTECTION FOR PARALLEL SWITCHES

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

FURKAN KARAKAYA

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

SEPTEMBER 2020

Approval of the thesis:

CHARACTERIZATION OF GAN TRANSISTORS AND DEVELOPMENT OF BI-DIRECTIONAL DC/DC CONVERTER WITH HALF-BRIDGE HAVING SHORT CIRCUIT PROTECTION FOR PARALLEL SWITCHES

submitted by **FURKAN KARAKAYA** in partial fulfillment of the requirements for the degree of **Master of Science in Electrical and Electronics Engineering Department, Middle East Technical University** by,

Prof. Dr. Halil Kalıpçılar
Dean, Graduate School of **Natural and Applied Sciences** _____

Prof. Dr. İlkay Ulusoy
Head of Department, **Electrical and Electronics Engineering** _____

Assist. Prof. Dr. Ozan Keysan
Supervisor, **Electrical and Electronics Engineering** _____

Examining Committee Members:

Assoc. Prof. Dr. Murat Göl
Electrical and Electronics Engineering, METU _____

Assist. Prof. Dr. Ozan Keysan
Electrical and Electronics Engineering, METU _____

Prof. Dr. Işık Çadırcı
Electrical and Electronics Engineering, Hacettepe University _____

Prof. Dr. Timur Aydemir
Electrical - Electronic Engineering, Gazi University _____

Assist. Prof. Dr. Taner Göktaş
Electrical and Electronics Engineering, İnönü University _____

Date: 11.09.2020

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Surname: Furkan Karakaya

Signature :

ABSTRACT

CHARACTERIZATION OF GAN TRANSISTORS AND DEVELOPMENT OF BI-DIRECTIONAL DC/DC CONVERTER WITH HALF-BRIDGE HAVING SHORT CIRCUIT PROTECTION FOR PARALLEL SWITCHES

Karakaya, Furkan
M.S., Department of Electrical and Electronics Engineering
Supervisor: Assist. Prof. Dr. Ozan Keysan

September 2020, 138 pages

Wide band-gap semiconductors are superior to Si-based semiconductors with their increased electron mobility and breakdown strength which leads to small package sizes, low parasitics, and increased switching frequency capability. Efficient and dense power converter could be obtained with wide band-gap devices especially GaN transistors. This thesis investigates the GaN HEMTs in terms of their characterization and application. The gate charge and output capacitance of GaN HEMTs are characterized by designed experimental setups and they are compared with manufacturer-provided data. The differences between outcomes and the datasheet are highlighted and explained. Based on the characterized elements of GaN HEMTs, their switching performance is studied within a simulation platform and effects of package capacitances, parasitic inductances, temperature, gate resistance are discussed. A half-bridge prototype design is performed where layout optimization is done for a parallel-connected GaN HEMTs. Moreover, a short circuit protection technique is implemented on the same half-bridge board to save GaN HEMTs from overcurrent and increase the reliability. The short circuit protection method is able to detect the fault in 40 ns and can

control the short circuit current in 100 ns. Lastly, an example application is realized with GaN HEMT based half-bridges to have a bi-directional DC/DC converter. The bi-directional DC/DC converter has 5.4 kW power rating with 5.24 kW/l power density. This power density is achieved with 450 kHz of switching frequency where zero voltage switching is applied with critical conduction mode switching. The efficiency of the converter is 97.7% at maximum load.

Keywords: Gallium Nitride, GaN HEMT, Device Characterization, Layout Design, Short Circuit Protection, Bi-directional DC/DC Converter

ÖZ

GAN TRANSİSTÖRLERİN KARAKTERİZASYONU VE PARALEL ANAHTARLAR İÇİN KISA DEVRE KORUMASINA SAHİP YARIM KÖPRÜ İLE ÇİFT YÖNLÜ DA/DA ÇEVİRİCİ GELİŞTİRİLMESİ

Karakaya, Furkan
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi: Dr. Öğr. Üyesi. Ozan Keysan

Eylül 2020 , 138 sayfa

Artırılmış elektron hareketlilikleri ve bozulma dayanımı seviyeleri ile geniş bant aralıklı yarı iletkenler Si tabanlı yarı iletkenlere göre daha üstünlerdir. Bu üstünlük yarı iletkenlerin küçük paketlerde üretilmesine, düşük parazitik oluşmasına ve anahtarlama frekansının artırılabilir olmasına olanak sağlar. Geniş bant aralıklı yarı iletkenler ile özellikle de GaN HEMT cihazlar ile yüksek verimli ve düşük hacimli güç çevricileri tasarlanılabilir. Bu tezde, GaN HEMT anahtarlar, nitelendirme ve uygulma çalışmaları ile incelenmiştir. Yarı iletken kapısının elektriksel yükü ve çıkış sığası, tasarlanmış deneysel çalışmalarla nitelendirilmiş olup üreticinin paylaştığı veri ile kıyaslanmıştır. Üretici verisi ile deneysel sonuçlar arasındaki farklar vurgulanmış ve bu farkların sebepleri irdelenmiştir. Nitelendirilen bu parametreler ile GaN HEMT cihazların anahtarlama performansları benzetim çalışmaları ile değerlendirilmiş ve paket sığası, parazitik endüktans,sıcaklık, kapı direnci gibi parametrelerden nasıl etkilendiği tartışılmıştır. Daha sonra hat tasarım eniyileştirme çalışması yapılarak paralel GaN HEMT kullanımı ile birlikte yarım köprü tasarımı gerçekleştirilmiştir. Bununla

beraber, GaN HEMT'leri yüksek akımdan korumak ve güvenilirliği artırmak için bir kısa devre koruma yöntemi aynı yarım köprü baskı devre kartı üzerine yerleştirilmiştir. Bu kısa devre koruma yöntemi, hatayı 40 ns içerisinde algılamakta ve 100 ns içerisinde kısa devre akımını kontrol altına alabilmektedir. Son olarak bir çift yönlü DA/DA çevirici örnek uygulaması tasarlanan yarım köprü baskı devre kartları kullanılarak gerçekleştirilmiş ve 5.24 kW/l güç yoğunluğuna 5.4 kW güç değeri altında ulaşılmıştır. Bu güç yoğunluğu sıfır gerilim anahtarlama uygulanarak çıkılan 450 kHz anahtarlama frekansı ile elde edilmiştir. Sıfır gerilim anahtarlamanın elde edim yöntemi kritik mod anahtarlamadır. DA/DA çeviricinin verimliliği tam yük altında %97.7 olarak ölçülmüştür.

Anahtar Kelimeler: Galyum Nitrat, GaN HEMT, Cihaz Karakterizasyonu, Hat Tasarımı, Kısa Devre Koruması, Çift Yönlü DA/DA Çevirici

To my lovely family...

ACKNOWLEDGMENTS

Firstly, I would like to express my sincere gratitude to Assist. Prof. Dr. Ozan Keysan for his continuance motivation, significant guidance, and endless encouragement. His continuous support helped me to stay productive always.

I would also like to express my gratitude to dear committee members: Prof. Dr. Işık Çadırcı, Prof. Dr. Timur Aydemir, Assoc. Prof. Dr. Murat Göl and Assist. Prof. Dr. Taner Göktaş for helping me to improve my thesis work. I am also grateful to Assist. Prof. Dr. Emine Bostancı for helping me to improve my power electronics background.

This thesis is composed not only with my effort but also with the help of my dear colleagues and friends. I would like to name them and their contribution one by one.

I have to thank Armin Jafari and Prof. Dr. Elison Matioli for their contribution in Chapter 2. My summer internship in Power and Wide band-gap Electronics Research Laboratory at EPFL was a breakthrough to develop my understanding of wide band-gap semiconductors. Dear Enes Ayaz and dear Goksu Kaval helped me a lot to reach out to the outcomes of this chapter as well. I am grateful for their supports and efforts.

Chapter 3 is a mutual work of me and Mesut Ugur whose support deserves a true appreciation. We spent two years together for the Integrated Modular Motor Driver project which taught a lot of things to both of us.

Chapter 4 could not be completed without kind helps of Ozturk Sahin Alemdar. It is always joyful to study on the same projects with him. I am so grateful for his technical supervision and support.

I am also eternally grateful to Emre Karabakla, Furkan Tokgoz, Gokhan Cakal, and Ozgur Gulsuna for their valuable time and help for the design and tests discussed in Chapter 5.

Moreover, I was involved in technical discussions for many times and learned lots of things from dear METU PowerLab and EPFL PowerLab members. Therefore, I would also like to express my pleasure to Göksenin Hande Bayazıt, Hakan Polat, Hakan Sarac, Mohammad Samizadeh Nikoo, Nail Tosun, Reza Soleiman Zadeh Ardebili, and Yusuf Basri Yılmaz.

I am thankful to TÜBİTAK, the Scientific and Technological Research Council of Turkey, for granting me their M.S. studies scholarship, BİDEB 2210. Also, I am grateful to TÜBİTAK for funding me as a researcher student for two years in the project, Development of 7.5 kW Integrated Modular Motor Drive with Permanent Magnet, 117E252.

I am also very grateful to my friends who always gave me strength with their support and friendship. When you live apart from your family, your friends become like your family, and I feel very lucky to have such a family.

And lastly, there are no words of thanks or gratitude that can represent my indebtedness to my mom, Nurcan Karakaya, my dad, Eyüp Karakaya, and my brother, Gürkan Karakaya and my family. I am deeply thankful for their unending support during my whole life.

TABLE OF CONTENTS

LIST OF TABLES

TABLES

LIST OF FIGURES

FIGURES

LIST OF ABBREVIATIONS

ABBREVIATIONS

GaN	Gallium nitride
Si	Silicon
HEMT	High electron mobility transistor
DC	Direct current
AC	Alternative current
WBG	Wide band-gap
SiC	Silicon carbide
AlGaN	Aluminium gallium nitride
2DEG	Two dimensional electron gas
MOSFET	Metal oxide semiconductor field effect transistor
d-mode	Depletion mode
e-mode	Enhancemenet mode
IC	Integrated circuit
SC	Short circuit
SCP	Short circuit protection
ZVS	Zero voltage switching
QSW	Quasi-square wave
ZVRT	Zero-voltage resonant-transition
DUT	Device under test
PCB	Printed circuit board
CSI	Common source inductance
EMI	Electromagnetic interference

GIT	Gate injected transistors
STO	Soft turn-off
HTO	Hard turn-off
CrCM	Critical conduction mode
PWM	Pulse width modulation
G	Gate
D	Drain
S	Source
SS	Kelvin source
DPT	Double pulse test
GND	Ground
FEA	Finite element analysis
PTC	Positive temperature coefficient
HSF	Hard switching fault
KVL	Kirchhoff's voltage law
μC	Micro-controller
EN	Enable
BJT	Bipolar junction transistor
CMTI	Common mode transition immunity
FFT	Fast fourier transform
DSP	Digital signal processor
TIM	Thermal interface material
LFM	Linear feet per minute
CFM	Cubic feet per minute
Q_T	High side transistor
Q_B	Low side transistor
MLT	Mean length turn

SMD	Surface mount design
TH	Through hole
GWHz	Gigawatt-Hertz

LIST OF VARIABLES

μ	Electron mobility
V_{ds}	Drain-to-source voltage
V_{gs}	Gate-to-source voltage
V_{gd}	Gate-to-drain voltage
C_{gs}	Gate-to-source capacitance
C_{gd}	Gate-to-drain capacitance
C_{ds}	Drain-to-source capacitance
C_{iss}	Input capacitance
C_{rss}	Transfer capacitance
C_{oss}	Output capacitance
Q_{gs}	Gate-to-source charge
Q_g	Gate charge
I_{ds}	Drain-to-source current
R_{ds-on}	On state resistance
R_g	Gate resistance
R_{ext}	External resistance
R_{int}	Internal resistance
P_g	Gate loss
$P_{R,ext}$	Loss on external gate resistance
P_{TR}	Loss on internal gate resistance
T_{TR}	Transistor temperature
P_{GD}	Loss on gate driver
T_{GD}	Gate driver temperature

V_{ON}	On state gate voltage
V_{OFF}	Off state gate voltage
V_{th}	Threshold voltage
f_{sw}	Switching frequency
Φ	Flux linkage
E_{oss}	Stored energy on output capacitance
L_g	Gate loop inductance
L_{sin}	Internal inductance of source pin
L_{din}	Internal inductance of drain pin
L_{gin}	Internal inductance of gate pin
R_{on}	Turn-on resistance
R_{off}	Turn-off resistance
R_{com}	Common resistance
T_j	Junction temperature
T_{amb}	Ambient temperature
L_{load}	Load inductance
I_{load}	Load current
V_{ch}	Channel voltage
I_{ch}	Channel current
t_{dead}	Dead time
C_{bypass}	Bypass capacitor
C_{bus}	DC-link capacitor
V_{bus}	DC-link voltage
f_{osc}	Oscillation frequency
L_{con}	Connection inductance
V_{sense}	Induced sense voltage
L_{sense}	Sense loop inductance

A_{sense}	Sense loop area
g_m	Trans-conductance
M	Mutual inductance
M_{PS}	Mutual inductance between power loop and sense loop
V_{ref}	Reference voltage
R_b	Base resistance
$\vec{B}$	Flux density
$\vec{B_{ac}}$	AC flux density
$\vec{B_{dc}}$	DC flux density
$\vec{B_{peak}}$	Peak flux density
I_{SC}	Short circuit current
$\vec{J}$	Current density
ϵ	Induced voltage
R_f	Filter resistance
C_f	Filter capacitance
V_{comp}	Comparator output voltage
V_{filt}	Filter output voltage
R_{J-C}	Junction to case thermal resistance
R_{TIM}	Thermal resistance of thermal interface material
R_{HS-A}	Heat sink to ambient thermal resistance
R_{total}	Total thermal resistance
A_{total}	Total TIM area
α_{TIM}	Thermal resistance per inch square of TIM
V_{IN}	Input voltage
V_{OUT}	Output voltage
ΔI_{cap}	The ripple current passing through output or input filter capacitor

$\hat{I}_{L,neg}$	Negative peak value of inductor current
ΔI_L	The ripple current passing through filter inductor
L_{gap}	Air gap length
A_e	Effective area
A_{wind}	Winding area
V_e	Effective volume
P_{ind}	Loss on inductor
P_w	Winding loss of inductor
P_c	Core loss of inductor
P_{dc}	DC winding loss of inductor
P_{ac}	AC winding loss of inductor
R_{dc}	DC winding resistance of inductor
R_{ac}	AC winding resistance of inductor
$\Re$	Reluctance
μ_o	Permeability of free space
N	Turns number
A_{wire}	Wire area
P_{sp}	Specific power loss of a core
$T_{winding}$	Winding temperature
T_{core}	Core temperature
P_{bridge}	Total power loss on GaN HEMTs of a half bridge board
P_{ref}	Reference power loss on GaN HEMTs of a half bridge board
T_{HS-op}	Operating temperature of heat sink
T_{HS-ref}	Reference temperature of heat sink
D	Duty cycle

CHAPTER 1

INTRODUCTION

The history of power electronics is merged into the history of power semiconductor technology when the first solid-state power semiconductor device is invented in the early 1900s. The most critical parameters of a power electronics product such as efficiency, size, and the range of the regulation capability are mostly limited with the capabilities of power semiconductors. Over the last 60 years, Silicon (Si) based power semiconductors dominated the field and led to a huge development in power electronics. In recent years, designers highly achieved the limits of Si power semiconductors and new types of semiconductors have been required to further improve power electronics technology. With their superior characteristics over Si, wide band-gap (WBG) semiconductors revived the hopes for better power electronics outcome. Silicon-carbide (SiC) and Gallium-Nitride (GaN) based power semiconductors are now available and they are highly addressed by different types of power electronics applications with tight requirements. This thesis focuses on particularly GaN power devices in terms of their characterization and applications.

In this chapter, the motivation and problem definition is given by citing former studies related to characterization and applications of GaN transistors. Then, the contribution of each chapter is explained in detail in an outline format.

1.1 Motivation and Problem Definition based on Literature Survey

Wide band-gap (WBG) transistors introduce significant improvement possibilities for power electronics applications. Either Silicon-Carbide (SiC) or Gallium-Nitride (GaN) has a wider band-gap in comparison to Silicon (Si) devices which leads to

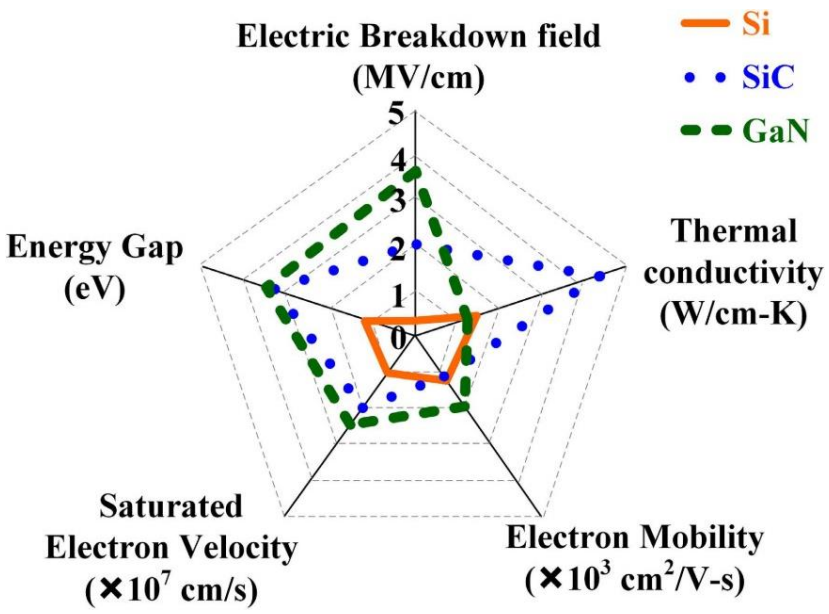


Figure 1.1: Comparison of Si, SiC, and GaN for power semiconductor applications [1]

smaller power semiconductors for the same voltage rating. The superior characteristic of WBG transistors is not limited to the high electric break-down field. A comparison scheme is presented in Fig. 1.1 where five different specifications are given for Si, SiC, and GaN material. High break-down strength of a device enables to make the device more compact [1]. As a result of compactness, the on-state resistance decreases, the parasitic in-package inductance decreases, the parasitic capacitance also decreases, so the switching speed of the device increases. Moreover, higher saturated electron velocity leads to better switching performance [1]. However, it is required to understand the characteristics of the GaN power device in more detail and required to verify the performance characteristics under different operating conditions such as different bias voltage levels and different junction temperatures.

The structure of the device is one of the most important parameters affecting the characteristics. In contrast to Si transistors which gain conductivity via doping regions, GaN transistors gain the conductivity via piezoelectricity. The crystal structure of GaN brings piezoelectric characteristics which help to achieve very high conductivity in comparison to other types of semiconductor materials [2]. A thin layer of AlGaN

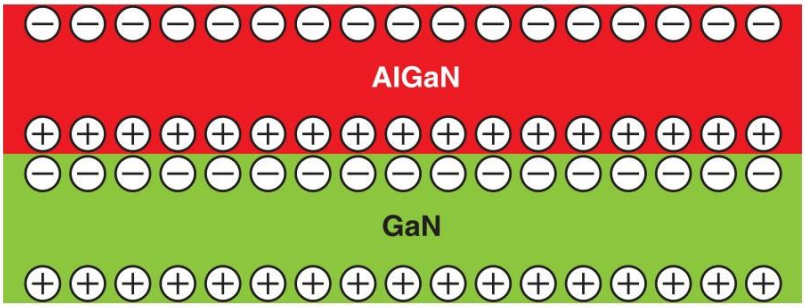


Figure 1.2: Simplified cross section of a GaN/AlGaN heterostructure showing the formation of a 2DEG [2]

on top of GaN crystal creates a strain at the contact region and accumulates negative charge which can move freely as given in Fig. 1.2. The accumulated negative charge is called two-dimensional electron gas (2DEG) and it is the reason behind high conductivity. Comparing the body diode of Si MOSFETs created by p-n junctions to the 2DEG of A GaN transistor, an electron can move in both directions in 2DEG. Therefore, GaN transistors do not include a body diode and do not suffer from weak points of body diodes like reverse recovery charge.

Since the GaN crystal is conductive through the interface with AlGaN, the 2DEG channel stays normally ON. In order to control the conductivity, a depletion-mode (d-mode) gate is placed on top of AlGaN material to deplete electrons accumulated in GaN crystal as shown in Fig. 1.3. The channel is not conductive as long as a negative bias is applied to the gate. However, due to reliability concerns, normally OFF transistors are preferred for power electronics applications. Normally OFF transistors under zero gate bias are known as enhancement-mode (e-mode) transistors. In order to have a normally OFF channel, a d-mode GaN transistor is connected in series with an e-mode Si MOSFET as presented in Fig. 1.4. This type of device is named Cascode GaN transistor and they are available on the market. It is advantageous to use Cascode GaN transistors as long as the bias voltage is higher than 200 V because the on-state resistance of Si MOSFET gets comparable with channel resistance of d-mode GaN transistor if the voltage rating is lower than 200 V [2]. Cascode GaN transistors are also advantageous with their inherent p-n junction at Si MOSFET. This p-n junction can be used as a free-wheeling diode with a lower forward voltage drop.

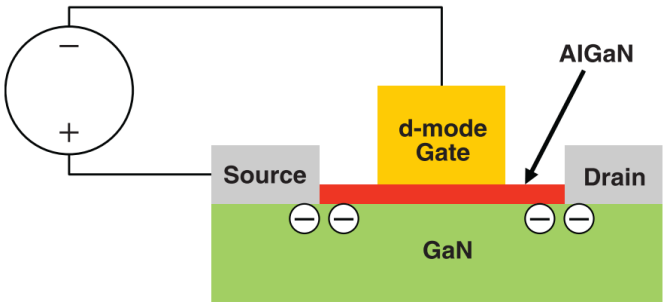


Figure 1.3: Control of the conductivity by a depletion-mode gate structure [2]

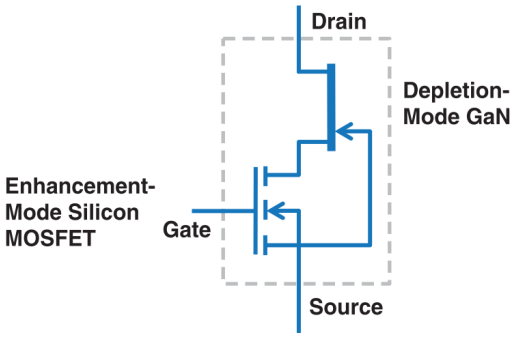


Figure 1.4: An e-mode Si MOSFET is connected in series with a d-mode GaN transistor [2]

Additionally, the gate threshold voltage for cascode transistors is the same with traditional levels, so it enables to use of regular gate-driver integrated circuits (ICs). However, the main problem of this type of device is the packaging [3]. In addition to power loop inductance, high package inductance is responsible for gate ringing [3], high voltage induction, high switching loss [1], and electromagnetic interference (EMI) problems.

Another way to get an e-mode gate structure is by having a pGaN gate. In this structure, a positively charged GaN layer is placed on top of the AlGaN layer as given in Fig. 1.5. The positive built-in voltage of the pGaN layer, i.e. threshold voltage, has to be overcome to get a fully conductive channel [2]. In this thesis, all of the studies are conducted with e-mode pGaN gated GaN High Electron Mobility Transistors (HEMTs). Transistors, GS66508T and GS66508B have 650 V, 30 A voltage and current ratings [4, 5].

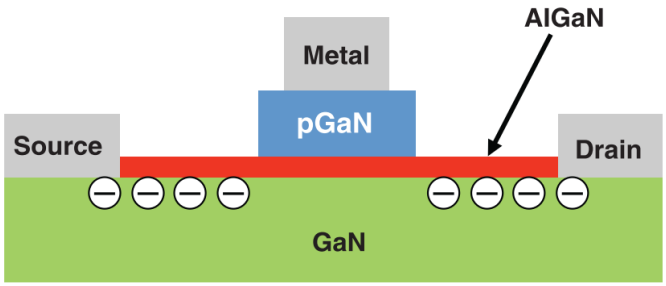


Figure 1.5: Normally OFF structure with a pGaN gate [2]

An important measure of transistor quality is being able to operate with the same characteristic though the varying operating conditions such as temperature and bias voltage change. Junction temperature is a key factor affecting the performance of GaN transistors. Even though the threshold voltage is relatively stable over temperature for GaN devices [1, 2], the electron mobility (μ) of e-mode GaN HEMTs decreases significantly with temperature, so the on-state resistance is degraded [3]. An increase in the on-state resistance could increase conduction losses and easily invalidate the thermal cooling design. However, under a short-circuit (SC) fault condition, an increase in on-state resistance can limit the peak of SC current which improves the SC ruggedness of GaN HEMTs [3, 6]. Similar behavior is observed in the breakdown mechanism as well. If the critical electric field is exceeded, the 2DEG is destroyed which results in a great increase in on-state resistance [2], i.e., open circuit.

In a like manner to junction temperature, the bias voltage is another key factor affecting device performance. The surface charge gets trapped near the drain edge of the gate terminal when the device stays in the OFF state with an applied drain-to-source bias voltage (V_{ds}). The trapped charge near the gate behaves as a virtual gate and weakens the 2DEG until they are released [1]. This phenomenon is called the current collapse and the degradation in on-state resistance is proportional to the applied voltage. It is reported that it takes too long time for charges to return to the initial state [7]. This problem should have been solved by the manufacturer of the device. For this purpose, the gate and source field plates are extended towards drain as shown in Fig. 1.6 to reshape electric field distribution so that a lower amount of charge is trapped near gate [1].

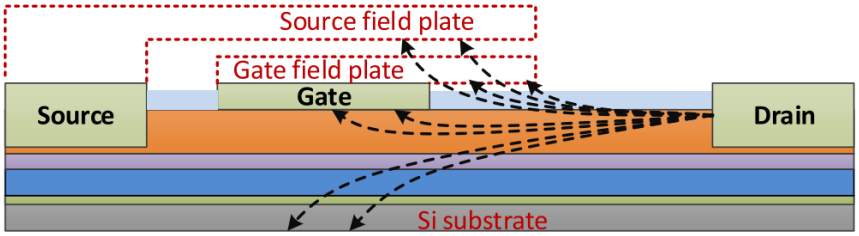


Figure 1.6: Redistribution of electric field with extended source and gate field plates [1]

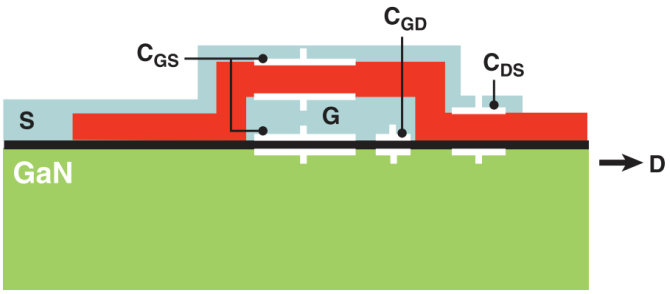


Figure 1.7: Source of the parasitic capacitances [2]

Extending and placing the plates affect the parasitic capacitances as well. Fig. 1.7 shows the source of parasitic capacitances. Those capacitances directly affect the switching characteristic and switching losses [8]. There would be no parasitic capacitance in an ideal case; however, the metal plates with the insulating material between them acts as a capacitor. For the minimization of package capacitance, the plates should be manufactured away from each other. The capacitors are shown in Fig. 1.7 affect switching characteristics differently. The input capacitance ($C_{ISS} = C_{GS} + C_{GD}$) changes the charging and discharging time constant of gate-source voltage, so the dead-time has to be selected accordingly. It also affects the gate loop design as will be discussed in Section 4.1. The output capacitance ($C_{OSS} = C_{DS} + C_{GD}$) slows down the transition, so increases the switching loss. The miller capacitance ($C_{RSS} = C_{GD}$) builds the feedback path from drain to the gate and unsuccessful designs can easily fail with a false turn-on fault [9] because of the miller capacitance.

The switching losses are not limited to the overlap losses during charging and discharging the output capacitance. As a matter of fact, the switching losses related

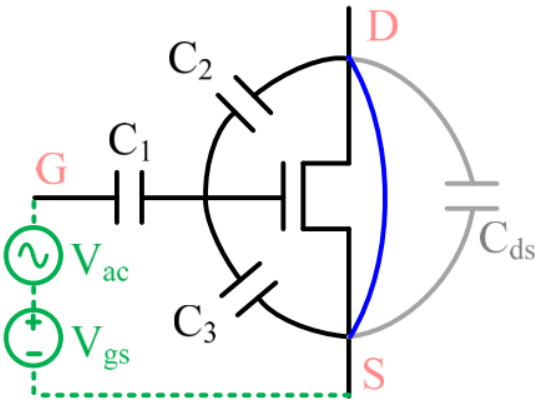


Figure 1.8: Characterization circuit for C_{iss} vs V_{gs} [12]

to output capacitance do not exist for zero voltage switching (ZVS) topologies [10]. For the applications where the switching frequency goes beyond 100 MHz [11], even though ZVS is applied, the loss caused by charging and discharging current of input capacitance gets effective. Even though the gate-source charge (Q_{GS}) is reported in datasheets, that charge is characterized for hard switching applications. A characterization method for input capacitance and miller capacitance is proposed in [12]. Utilizing a DC bias and a high-frequency (> 1MHz) AC supply as shown in Fig. 1.8, the impedance can be characterized by measuring the AC current. This technique is complicated with the requirement of various supplies and measurement tools. A simple method based on small-signal input capacitance measurement is proposed by the author *et al.* in [13] as will be discussed in Chapter 2.

On the other hand, the characterization of output capacitance might be challenging with conventional methods. Sawyer-tower is a common method to measure output capacitance of devices [14, 15]. The device-under-test (DUT) is connected in series with a reference capacitor and a large sinusoidal voltage is applied. Basically, the voltage ratio gives the capacitance of the device. However, it is hard to capture nonlinear output capacitance of a device with only one reference capacitor [16]. A method is proposed in [16] which utilizes the resonant charging of the output capacitor of the device with the help of an inductor. The same method is applied in this thesis on GS66508T GaN HEMT to characterize output capacitance.

Having characterized the required parameters, it is also important to build a model

to evaluate device performance. Simulation models are necessary to analyze switching performance and losses of the device before implementation. Investigation of the switching behavior of GaN power FETs is important for several reasons. First, the high switching speed of GaNs makes them more vulnerable to di/dt, dv/dt effects, and parasitic components. Secondly, e-mode GaNs have reverse conduction capability without an intrinsic or external diode [17]. They act as a resistor just like MOSFETs in forward conduction mode; however, their behavior in reverse conduction mode is different from the forward conduction, varying with the applied gate-source (V_{gs}) voltage. Therefore, turn-on and turn-off characteristics are dependent on applied gate-source voltage. In half-bridge configurations, a negative gate voltage is usually required to avoid false turn-on, which results in a much higher on-state voltage when the device is not actively turned-on during dead-time [9]. Another reason for studying the switching behavior of GaN is that their switching loss and reverse conduction loss model are not the same as Si MOSFETs. Although the dead-time period and its effects on power loss calculations are usually ignored in other applications, it may affect the converter efficiency significantly in e-mode GaN applications [9].

Several studies have been published regarding e-mode GaN FET modeling. In [18], the (I_{ds} - V_{ds}), (I_{ds} - V_{gs}) characteristics and dynamic on-state resistance (R_{ds-on}) behavior of e-mode GaNs are obtained using curve fitting from experimental data. An analytical model is applied for steady-state behavior with temperature dependency and for the dynamic response with varying input and output capacitances in [19]. A mode-by-mode analysis is investigated in [20] for estimating the switching losses under various parasitic effects using small-signal models. The false turn-on phenomenon and its relationship with the applied V_{gs} voltage are investigated in [9]. Several methods have been proposed for the minimization of the reverse conduction losses such as using a Schottky diode in parallel with the synchronous GaN transistor [9].

Characterization of the device is not sufficient to ensure device behavior because the switching performance is also related to circuit dynamics. The layout parasitics on a printed circuit board (PCB) can increase the switching losses [1] and even can cause a short circuit fault [9]. The two most important loops on a layout are the power loop and the gate loop. Slow transition and voltage overshoot across drain-source termi-

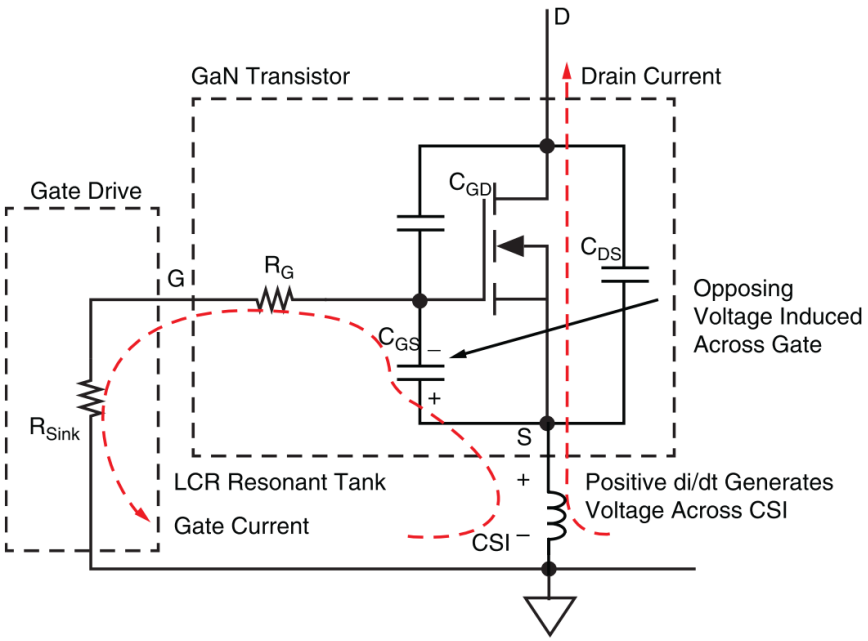


Figure 1.9: CSI causes oscillation on gate under high dI/dt [2]

nals are two main disadvantages of power loop inductance [2]. Similarly, gate loop inductance is responsible for gate voltage oscillation. An oscillation in V_{gs} voltage causes an oscillation in the trans-conductance of the device. Therefore, the device current oscillates and results in EMI problems. Also, high gate loop inductance is the main reason for false turn-on fault [9]. Another important parasitic is the common source inductance (CSI) which is the path shared by both the gate loop and the power loop [2] as given in Fig. 1.9. The CSI makes both the power loop and the gate loop worse. Additionally, it makes the gate loop sensitive towards a high dI/dt of drain current. In order to overcome the problems caused by CSI, a secondary source pin as known as Kelvin Source has been utilized in some transistors [1]. Separating source terminals for the gate loop and power loop helps to achieve minimum CSI.

It is sometimes necessary to connect transistors in parallel to increase current capability and also for better heat flux distribution on a heat-sink, where all paralleled devices are mechanically assembled [21]. However, parasitic inductance gains much more importance when device paralleling is applied. The undesired effects of parasitic inductances ease for soft switching applications. The loss distribution among paralleled devices occurs with respect to their on-state resistance [22] for soft switching cases. On the contrary, parasitic inductances are extremely effective for loss distribution and

operation safety of hard switching applications [23]. The minimization of parasitic inductances is not enough for paralleling applications. Parasitic inductances also have to be evenly distributed among parallel-connected switches [23, 24]. A 10 nH difference in power loop and gate loop inductances can cause 30% unbalance on current [25]. Thanks to the positive temperature constant of GaN HEMTs [3], parallel GaN transistors are able to self-regulate which needs to be assisted by careful design.

The proper design has to be reliable in terms of thermal loading and fault tolerance. GaN HEMTs have superior performance in comparison to Si and SiC devices. However, the reliability of GaN HEMTs is weak in comparison to other transistors in terms of their short-circuit (SC) ruggedness. The critical SC energy of p-GaN HEMTs is 2-3 times lower than cascade GaN transistors and 30 times lower than SiC MOSFETs [3, 26]. In addition, GaN HEMTs are extremely susceptible to circuit noise due to their low threshold levels [27]. This sensitivity requires a very careful layout design in order to eliminate the risk of false turn-on, [9], which can trigger an SC fault.

In order to maintain safe operation, a fast and reliable SC detection method is necessary. The protection technique should be capable of detecting the fault and clearing it in less than 500 ns if the DC bus voltage is higher than 350V [28]. There are several methods reported in the literature satisfying these requirements.

The most common method is adding a series resistor or a current sensor in series with GaN HEMTs to follow SC current [29]. A series resistor should be small enough to minimize power loss but in this case, the sensed voltage gets lower and can be distorted easily [27]. The current sensors are not practical because they do not have enough current range or enough bandwidth for SC detection [30]. Also, adding a component in series increases the power loop inductance and reduces the switching performance [6].

Another method commonly referred to is the desaturation technique which is used for sensing drain-source terminal voltage of GaN HEMTs. This technique suffers from its long settling time [6, 29, 31, 32]. Moreover, the diodes add capacitive loading in parallel with the output capacitance of transistor and it increases the switching losses [31]. Lastly, due to the high-temperature dependence of conductivity [3], it is hard to set a reference level for the desaturation technique [30].

Developed solutions are proposed in [6, 28, 31, 33]. The relation between gate current and drain current of GaN Gate Injected Transistors (GITs) is used for detecting SC fault in [31]. However, this is not applicable for GaN HEMTs because of their voltage driven gate structure. In [28], a sharp decrease in by-pass capacitors voltage is detected for identifying SC fault and the desaturation technique is applied to verify it. However, this method is incapable of detecting SC for variable DC voltages and it includes the disadvantages of desaturation technique such as increased output capacitance. In both [6] and [28], a soft turn-off (STO) mechanism is successfully adapted to prevent GaN HEMTs from an over-voltage breakdown risk. In [6], the drain-source voltage is sensed similar to the desaturation technique which has similar disadvantages: increased output capacitance and relatively hard identifiable threshold levels due to temperature dependency. In [33], a discrete protection circuit similar to [6] is proposed for GaN HEMTs with specific dual-gate pads. The dual-gate pads are utilized for the gate driver circuit and soft turn-off circuit separately for the relaxation of space limitations on PCB design.

Another technique is sensing the voltage on the PCB layout inductance induced by high dI/dt of the SC current. It is capable of detecting SC fault faster than the desaturation method and as a result, the maximum fault current is reduced by almost 20% [34]. This method is applied in [35] by the authors on a simple prototype and it is capable of detecting the fault in a couple of dozen nanoseconds. However, sensing the voltage across an inductance arises the suspicion of increased layout parasitics and sensing the voltage across a common source inductance like in [30] is criticized for deteriorating the layout parasitics, [6].

Moreover, few publications are focusing on the SC faults for parallel connected devices. In [36], the effect of parameters such as gate resistance and common source inductance over current sharing of parallel-connected IGBTs are discussed for hard switching fault (HSF) and fault under load (FUL). In [37], the gate oscillation of parallel-connected Si and SiC MOSFETs during the turn-off under an SC fault is investigated. It is pointed that the gate oscillation between parallel-connected transistors could reshape the unbalance of current sharing or even cause a false turn-on. This might be a concern for parallel-connected GaN HEMTs unless a soft turn-off is applied to remove SC fault.

In this thesis, a similar method to [35], sensing the voltage across by layout inductance is applied on a more developed half-bridge design where transistor paralleling is also applied for high-power applications. The design is discussed in detail in Chapter 4.

Even though it is possible to construct many different topologies with the half-bridge board, an example design of a bi-directional DC/DC converter application is performed where the maximization of power density is aimed. The bi-directional DC/DC converters are widely used as an interface for energy storage systems like batteries for applications such as telecom, automotive, and space [38, 39]. Based on the requirement of the application, the bi-directional DC/DC converter can be selected as an isolated or non-isolated topology. Unless the galvanic isolation is a must for the operation, the non-isolated topologies are more advantageous in terms of simplicity, cost, and the number of components [38, 40].

Further, today's trend with increasing demand is having compact, lightweight, small-sized power converters that give no option but increasing the switching frequency [41]. However, the increased switching frequency results in higher switching losses, reduced efficiency [41], and more importantly increased cooling component size. In order to overcome these problems, zero voltage switching (ZVS) turns into a must for bi-directional DC/DC converters.

The most common non-isolated bi-directional DC/DC converter is the buck/boost type converter with synchronous (synch.) switching. The high efficiency and simple structure of this topology [42] draw the attention. However, the most limiting factor of the synchronous buck/boost converter is the reverse recovery losses of the synch. switch's body diode especially for higher voltage applications. For example, synch. switches are hardly found in applications with 200 V and higher voltage ratings since the reverse recovery causes much more losses for higher voltage ratings [43]. The problem of reverse recovery is the stepped-up switching current of the main switch and also synch. switch and electromagnetic interference (EMI) caused by a sharp increase of reverse recovery current [41, 43, 44].

In order to deal with the reverse recovery phenomenon, ZVS can be implemented as it was required for high-frequency applications where compactness of the converter is aimed. The ideal switching operation is: all switches' body diodes conduct prior to

turn-on of the switches' channels, and all switches turn off with inductive load instead of capacitive load [43]. Fortunately, GaN HEMTs are now available on the market and they do not suffer from reverse recovery. However, the increase in switching frequency is still advantageous for compactness, so ZVS is required even for GaN HEMTs to reduce cooling component size.

There are three main methods for achieving ZVS on a bi-directional DC/DC converter. Adding extra active components for having resonant tanks, utilizing quasi or multi resonant converter at the cost of high peak voltage stress over switches, and lastly, lowering the inductance so that the inductor current can flow in both direction in a switching cycle and charges/discharges output capacitance of switches [38]. The last method is also called the quasi-square wave (QSW) ZVS method. In this thesis, the ZVS is achieved with the QSW ZVS method.

In the literature, achieving soft switching with low inductance is well discussed with pros and cons. Firstly, having low inductance results in increased current ripple, i.e. at least twice the average current, which causes much more conduction losses [38, 39, 44, 45]. A more circumspect solution would be preferring critical conduction mode (CrCM) switching where the main switch is turned on when the inductor current crosses the zero. The main disadvantage of the CrCM is the requirement of a long resonant period which limits the increase in switching frequency. Nevertheless, a coupled inductor design would help to increase resonant current so that the resonant period shortens. A well-prepared design where coupled inductors are used for CrCM switching with GaN HEMTs is presented in [39] for 1.2 kW application at 1 MHz switching frequency. Moreover, it is still possible to apply quasi-square wave (QSW) ZVS at the cost of high current ripple [43]. [45] utilizes QSW ZVS; in other words, zero-voltage resonant-transition (ZVRT), for a GaN HEMT based 25 W converter application at 3 MHz switching frequency. Additionally, even though it is a different topology aiming DC to AC conversion, the finalist applications of the Google Little Box challenge were using dual-buck H-bridge topology where ZVS is similarly achieved by allowing negative valley current [46].

In this thesis, a 5.4 kW bi-directional DC/DC converter with QSW ZVS is designed with GaN-based half-bridge prototypes. The converter utilizes two half-bridges to

cancel out inductor current ripple so that output voltage ripple and capacitor ESR losses [45] would be reduced.

1.2 Outline of Thesis and Contributions

Chapter 2 proposes a simple method to characterize the gate charge for soft switching applications. The characterized gate charge is compared with the charge reported in the datasheet and with the exact value derived by thermal experiments. It is shown that the gate charge deviates from datasheet values under a soft-switching situation. Furthermore, the output capacitance of a GaN HEMT is characterized and compared with datasheet value. Five different samples have been measured by the proposed method and the effect of output capacitance on switching losses is discussed.

In Chapter 3, a hybrid model has been proposed for the investigation of steady-state behavior and the switching transients of e-mode GaN power FETs. The state trajectories of the device during the turn-on and turn-off periods are obtained. The active turn-on and passive turn-on characteristics of the device are investigated on a double pulse test circuit. The effect of varying device capacitances and parasitic inductances on these trajectories and their possible outcomes are studied. In addition, the effect of the temperature and circuit parameters on the turn-on and turn-off characteristics are investigated.

Chapter 4 points out the importance of careful layout design for the power loop and the gate loop. Additionally, the layout design requirements for parallel-connected transistors are discussed. A practical example is given where the optimization of layout parasitics is performed using finite-element-analysis tools. Moreover, a novel short-circuit (SC) protection method is proposed and experimentally verified. The proposed ultra-fast SC protection technique is implemented on an industrial level half-bridge design where transistor paralleling is applied. Lastly, thermal design is performed to obtain maximum power density on the same half-bridge board. The designed half-bridge boards can be adapted to a different type of applications easily.

In Chapter 5, a bi-directional, zero-voltage resonant-transition (ZVRT) based DC/DC converter is implemented with designed half-bridge boards. The DC/DC converter

pushes the limits of GaN HEMTs with 400 V input voltage level where the switching frequency goes up to 450 kHz. The total power rating is around 5.4 kW and the power density is measured as 5.24 kW/l. Moreover, high ripple current introduced by the nature of quasi-square wave zero voltage switching is managed by interleaving. Careful magnetic design has been performed to overcome losses on filter inductors caused by high ripple and high frequency.

Finally, Chapter 6 explains the outcome of each chapter and gives the conclusion.

CHAPTER 2

GATE CHARGE AND OUTPUT CAPACITANCE CHARACTERIZATION

Being a novel device, Gallium-Nitride (GaN) High Electron Mobility Transistors (HEMTs) are subject to many types of tests to understand the nature of these devices more clearly. Even though manufacturers are publishing characteristics of a device, the data is valid only for certain conditions. Therefore, it might be necessary to characterize the device for sophisticated designs where the data-sheets do not provide all information.

In this chapter, the characterization of gate charge and output capacitance of GaN HEMT are studied. The datasheet provided gate charge value is valid only for hard switching cases and it might deviate from the actual one for soft or quasi-soft switching applications. Besides the gate charge, output capacitance is often characterized by impedance matching. Implementation of an alternative solution is given where output capacitance of a GaN HEMT is measured with a method based on nonlinear resonance [16]. These two characterization techniques are applied on a GaN HEMT, GS66508T (650V, 30A) device of GaN Systems.

2.1 Gate Charge Characterization

There are losses on a switching device caused by the conduction or the switching. Most of the time switching losses are calculated for drain-source current and voltage waveforms. In order to clear off these switching losses, soft switching topologies are used. However, for GaN HEMTs, the frequency of switching can rise up to several dozens of MHz range for a low power soft switching application and it can go beyond 100 MHz for Class type amplifier applications [11]. In this case, the losses on the

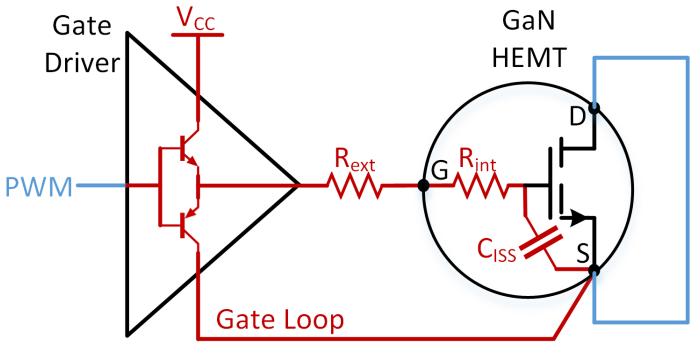


Figure 2.1: Push-pull type gate driver connected to GaN HEMT

gate might also be effective because of the increased switching frequency. The gate loss of a GaN HEMT can be estimated by using gate charge (Q_g) if the gate loop is modeled with a voltage supply, path resistance, and gate capacitance as given in Fig. 2.1. Instead of using the gate charge in the datasheet, the gate charge can be extracted by the integration of small-signal capacitance over the gate voltage as shown in (2.2). For this purpose, the small-signal capacitance is measured at 1 MHz by an impedance analyzer E4990A as presented in Fig. 2.2. For a hard-gating (push-pull) type gate driver operation, total gate loss (P_G) is the sum of the power losses on gate driver (P_{GD}), on external gate resistance ($P_{R,ext}$) and on internal gate resistance (P_{TR}) as given in (2.3). While the losses on the gate driver and external gate resistance heat up the ambient, the power loss on internal gate resistance heats up the transistor directly. In order to find internal gate power loss of the transistor, a thermal analysis has been accomplished and the results of three methods are compared for the total loss.

$$P_G = Q_G(V_{ON} - V_{OFF})f_{sw} \tag{2.1}$$

$$Q_G = \int_{V_{OFF}}^{V_{ON}} C_{ISS}(v)dv \tag{2.2}$$

$$P_G = P_{GD} + P_{R,ext} + P_{TR} \tag{2.3}$$

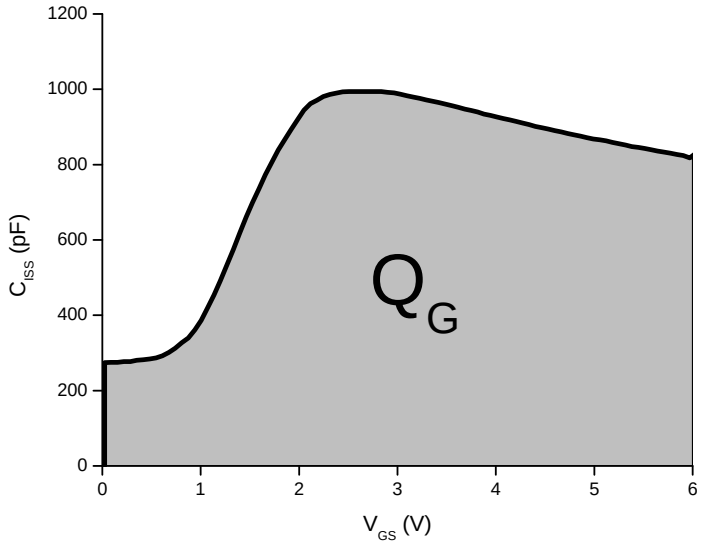


Figure 2.2: Input capacitance of GS66508T over gate-source voltage

2.1.1 Extracting Gate Loss

In order to find the gate loss of the transistor, it is switched on and off at high frequency with 0Ω external gate resistance by using a gate-driver integrated circuit (IC), LMG1020 [47], while keeping drain-source as short-circuited to have a soft-switching situation. Since there is no external gate resistance, the gate loop is highly susceptible to parasitic inductance. Therefore, the gate driver IC and the transistor should be placed as close as possible as shown in Fig. 2.3 where only two lossy components exist in the middle region: the transistor and the gate driver IC. This region is separated from the outer part of the PCB with tiny gaps to eliminate heat leakage towards outside. It is necessary to identify the losses on each component to find actual gate loss in the transistor. For this purpose, the two-port thermal network given in Fig. 2.4 should be identified.

In order to identify the two-port network, each power loss sources are activated one by one and for each case, the temperatures of transistor and gate driver noted by a high-resolution thermal camera, InfraScope^{TM} 2D MWIR-512 as presented in Fig. 2.5. The goal is to characterize the power losses of each component when their temperature is recorded simultaneously. For this purpose, in the first step, the gate driver

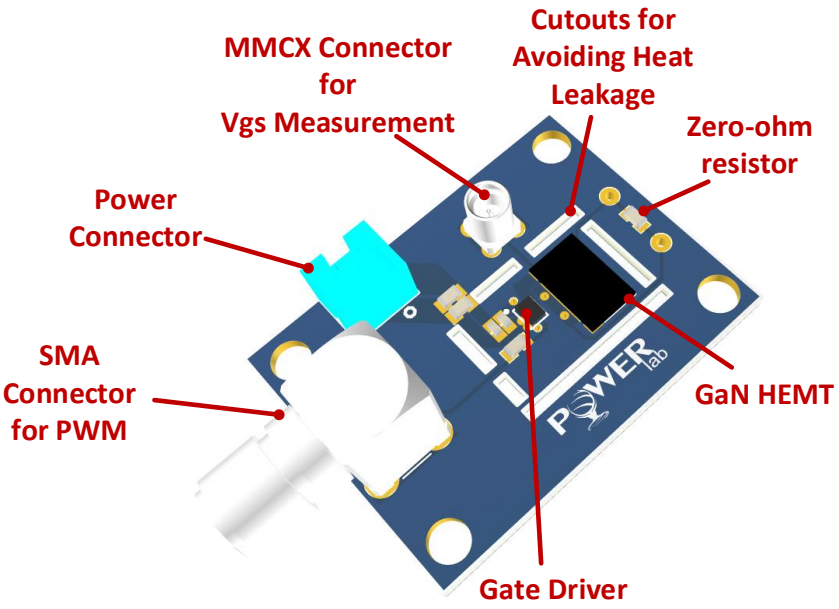


Figure 2.3: Gate loss characterization PCB

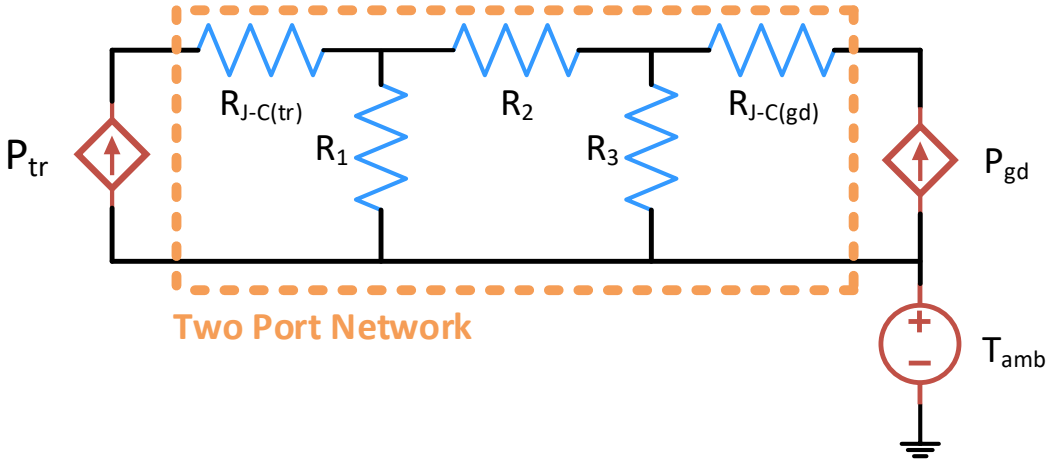


Figure 2.4: Thermal Network on the gate loss characterization PCB

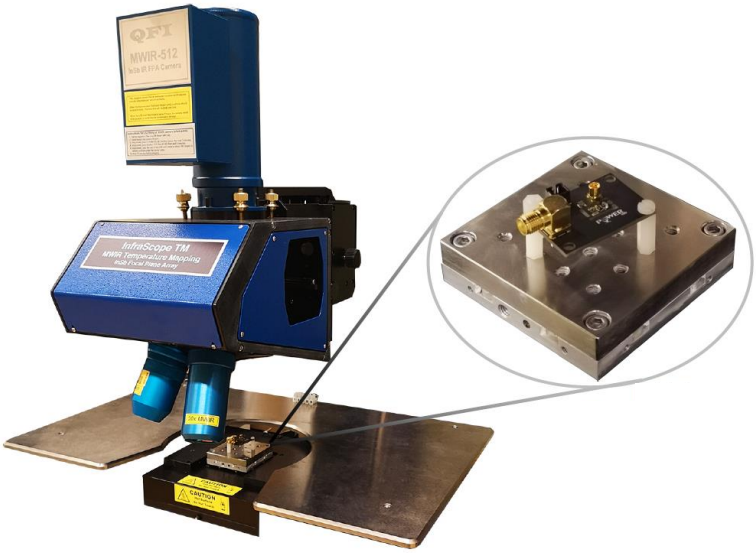


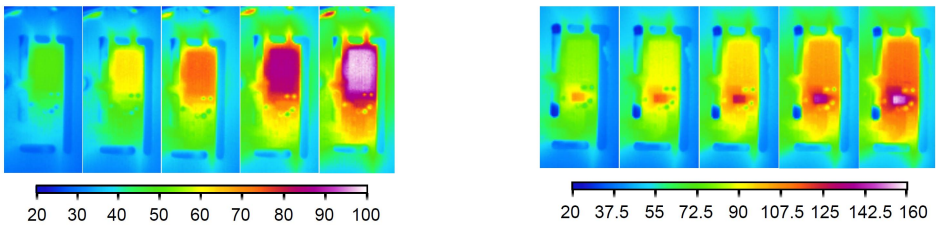
Figure 2.5: InfraScope 2D MWIR-512 thermal camera and gate loss characterization PCB connection

output is kept in the low state and the transistor is reverse biased to create some losses on the transistor. Then, the case temperature of the gate driver IC and the transistor is recorded as in Fig. 2.6 (a). In the second step, the gate driver output; in other words, gate-source terminals of the transistor are shorted. Then, the case temperature of the gate driver IC and the transistor is recorded again, Fig. 2.6 (b). Based on the results, thermal network matrix is characterized as given in (2.4) where R_{11} is 174 $°C/W$, R_{12} is 120 $°C/W$, R_{21} is 120 $°C/W$ and R_{22} is 162 $°C/W$. With this characterized two-port network it is possible to estimate power losses of each component using (2.5) if the temperature is known for both the transistor and the gate driver.

$$\begin{bmatrix} T_{tr} - T_{amb} \\ T_{gd} - T_{amb} \end{bmatrix} = \begin{bmatrix} R_{11} & R_{12} \\ R_{21} & R_{22} \end{bmatrix} * \begin{bmatrix} P_{tr} \\ P_{gd} \end{bmatrix} \tag{2.4}$$

$$\begin{bmatrix} P_{tr} \\ P_{gd} \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} * \begin{bmatrix} T_{tr} - T_{amb} \\ T_{gd} - T_{amb} \end{bmatrix} \tag{2.5}$$

Having characterized the two-port network of thermal resistances, the transistor is



(a) Power loss on the transistor

(b) Power loss on the gate driver

Figure 2.6: Heat distribution over PCB when individual losses are applied on GaN HEMT and gate driver

switched between 0 and 5 V drive levels with a high-frequency PWM signal where an example waveform is illustrated for 5 MHz in Fig. 2.7. As a result of switching, the losses are created on the transistor and the gate driver IC. These losses are characterized by measuring the temperatures and they are given in Fig. 2.8 with respect to the switching frequency.

2.1.2 Comparison and Discussion

In this study, three different methods are proposed to estimate transistor gate loss. First method is to use (2.1) with the measured gate charge given in Fig. 2.2. In the second method, the gate loss is identified by a thermal calibration. The last method calculates gate power loss using (2.1) with the datasheet provided gate charge value. The results of these three methods for 5 MHz switching frequency with 0-6 V drive levels and corresponding gate charges are presented in Table 2.1. Since the thermal calibration method is verified for different switching frequencies with different transistors, it is considered as the most accurate method. Taking this method as the reference, the first method deviates 4.9% which is almost three times lower than the deviation of the third method. It is because the gate charge (Q_G) given in the datasheet is characterized for hard switching cases where V_{DS} is charged up to 400 V [4]. Clearly, the equivalent gate charge for a soft-switching case is not identical to the hard switching.

Moreover, even though the second method, i.e. thermal calibration, is the most accurate technique, considering the simplicity, the first method is the most preferable way

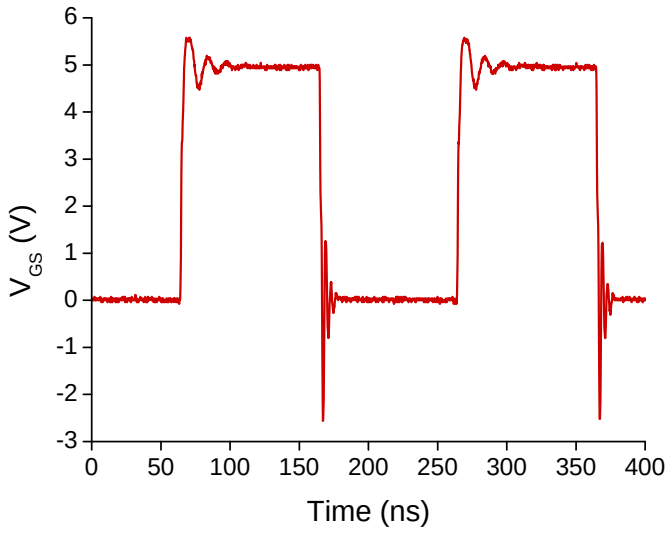


Figure 2.7: Gate-source voltage waveform at 5 MHz switching frequency

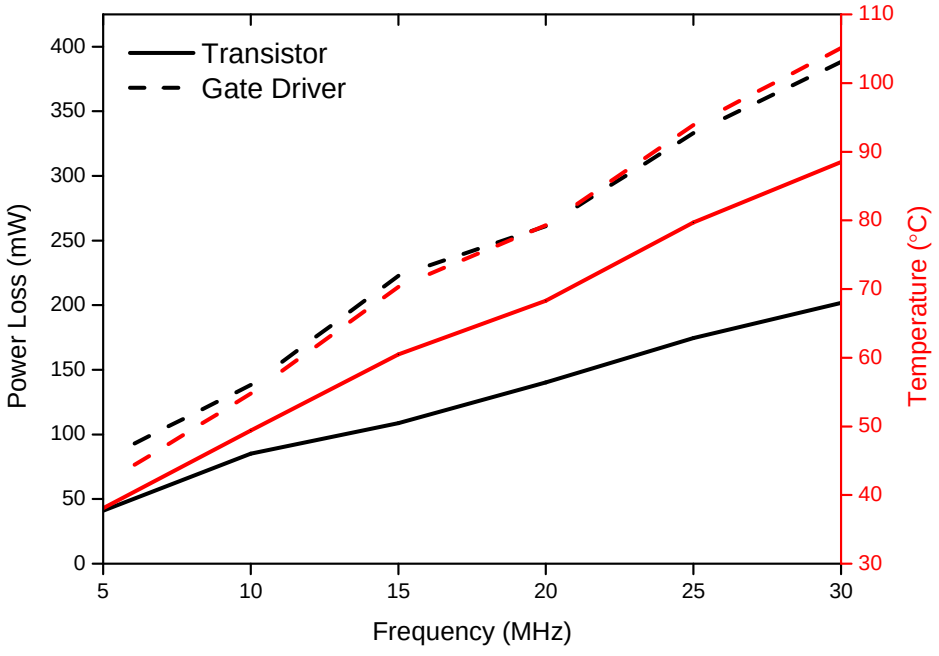


Figure 2.8: Power losses and resulting temperatures of the transistor and gate driver

Table 2.1: Comparison of three different gate loss estimation method

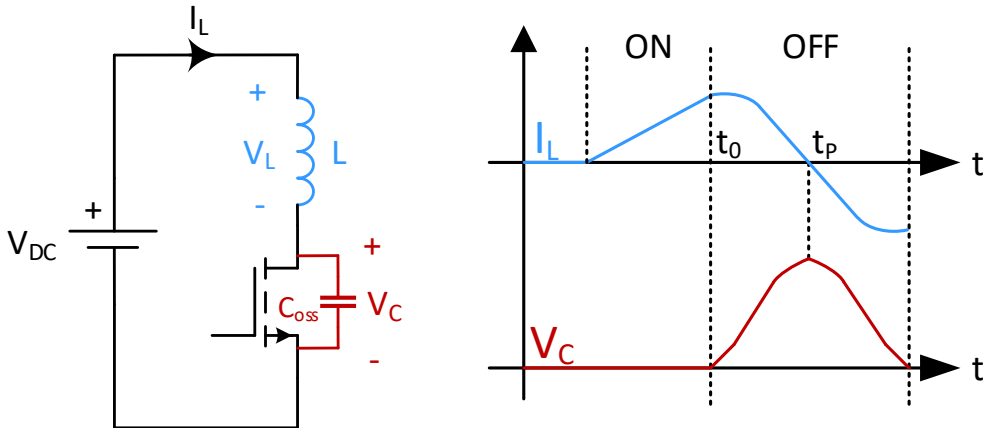
	First method	Second method	Third method
Charge extraction	Impedance analyzer	Thermal test	Datasheet
Gate charge (Q_G)	4.66 nC	4.9 nC	6.1 nC
Gate loss (P_G) @ 5 MHz	140 mW	147 mW	183 mW
Percent deviation	4.9%	0%	24.5%

to estimate gate loss of a GaN HEMT under soft-switching condition. The results also show that only one-third of total gate loss heats up directly the transistor while the remaining part dissipates on the gate driver and heats up the gate driver IC and ambient.

2.2 Output Capacitance Characterization

Output capacitance is a measure of transition speed or switching losses for a transistor. Even though it is not placed in the transistor intentionally, the metal contacts of drain, source and gate terminals and the electric field between them create a parasitic capacitance which slows down the transition. Since this capacitance does not stay constant with varying voltage, it is important to characterize output capacitance (C_{oss}) for estimating switching losses.

Manufacturers provide the required data and plots regarding C_{oss} by implementing the Sawyer-Tower electrical measurement method [14, 15]. A high amplitude sinusoidal voltage is applied to the device and a reference capacitor is connected in series with the device. It is aimed to have a reference capacitor such that the device and the capacitor have the same charges. Therefore, the selection of a suitable reference capacitor is essential. However, nonlinear change of the C_{oss} overvoltage cannot be met by the reference capacitor since its capacitance also varies with the temperature and voltage. In this section, a new C_{oss} measurement technique is based on the resonance of a series-connected inductor with the output capacitance, which is applied successfully in [16], is implemented for characterization of C_{oss} of GS66508T GaN HEMT.



(a) Circuit (b) Waveform

Figure 2.9: Output capacitance characterization circuit and illustrative waveform

2.2.1 Theory of Output Capacitance Characterization

Instead of using an external high voltage supply, the output capacitor (C_{OSS}) is charged by resonating an inductor that is connected in series with the device as shown in Fig. 2.9 (a). A small DC voltage (<1V) supply feeds the inductor current when the device is turned on. Whenever the device is turned-off, inductor current charges the output capacitance which can reach high voltage easily as illustrated in Fig. 2.9 (b). By measuring the voltage on the device, the output capacitance can be characterized by using circuit parameters.

Inductor current formula is given in (2.6) where I_o is the peak current that inductor reached when it was charged. This equation can be turned into (2.8) by using (2.7) which is valid where $V_{DC} << V_C$.

$$I_L(t) = I_o + \frac{1}{L}\int_{t_o}^{t} V_L(t)dt \tag{2.6}$$

$$V_L(t) = V_{DC} - V_C(t) \cong -V_C(t) \tag{2.7}$$

$$C_{OSS}(V_C)\frac{dV_C(t)}{dt} = I_o + \frac{1}{L}\int_{t_o}^{t} -V_C(t)dt \tag{2.8}$$

By manipulating the Lenz's Law (2.9) using (2.7), the flux on the inductor can be linked with the output capacitor voltage. The differential form in (2.9) can be replaced by an integration as given in (2.10) where total flux linkage ($\Psi(t_o)$) equals to LI_o. As a result, (2.8) turns into output capacitance equation (2.11) by using (2.10).

$$V_C(t) = \frac{d\Psi}{dt} \tag{2.9}$$

$$LI_o = \int_{t_o}^{t_p} V_C(t) \tag{2.10}$$

$$C_{OSS}(V_C) = \frac{\int_{t_o}^{t_p} V_C(t) - \int_{t_o}^{t} V_C(t)dt}{L\frac{dV_C(t)}{dt}} \tag{2.11}$$

2.2.2 Experimental Results of Output Capacitance Characterization

In order to verify the theory, a PCB is designed for output capacitance characterization as presented in Fig. 2.10. An inductor, 74437529203151 [48], with 150 μH inductance is connected in series with GS66508T GaN HEMT. The inductance is charged for 195 μs under 530 mV DC bias. Turning-off the transistor, drain-to-source voltage is charged by resonance up to 550 V as shown in Fig. 2.11.

The tests are conducted for 5 different samples and the characterized capacitances are given in Fig. 2.12. The results match with the datasheet information, [4], where the differences are observed sample to sample.

The output capacitance of the device is charged and discharged in each cycle. The energy stored on the output capacitance creates power loss for hard switching applications. This energy can be calculated by (2.12). The stored energy (E_{OSS}) is calculated using C_{OSS} vs V_{DS} plots for five samples and the datasheet as given in Fig. 2.13. In addition, the reported E_{OSS} as 8 μJ in the datasheet for 400 V is also marked on the figure 2.13. The integrated energy of the datasheet waveform deviates from samples as voltage gets higher. Moreover, the reported energy for 400 V in the datasheet does not match with the integrated energy of the datasheet capacitance waveform. Con-

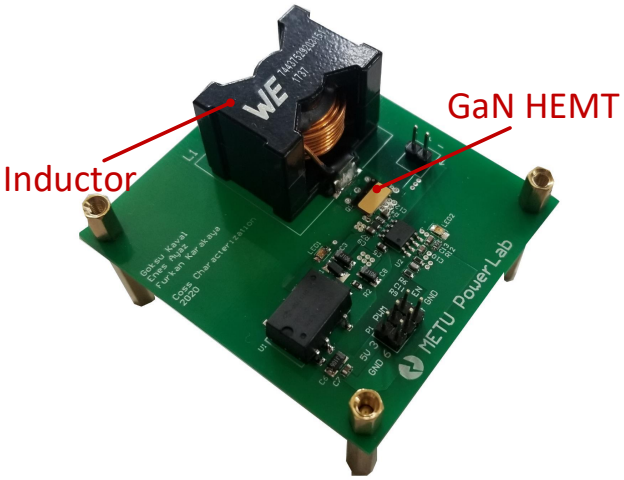


Figure 2.10: PCB designed for output capacitance characterization of GS66508T GaN HEMT

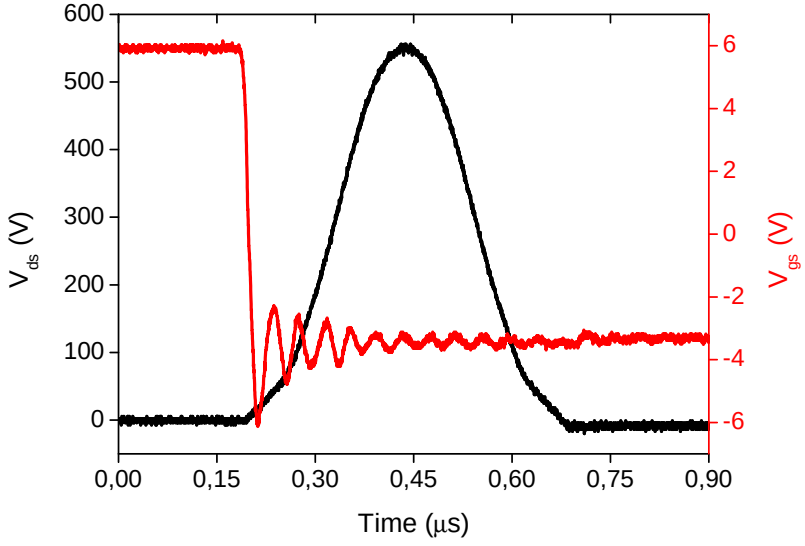


Figure 2.11: Experimental results of output capacitance characterization tests

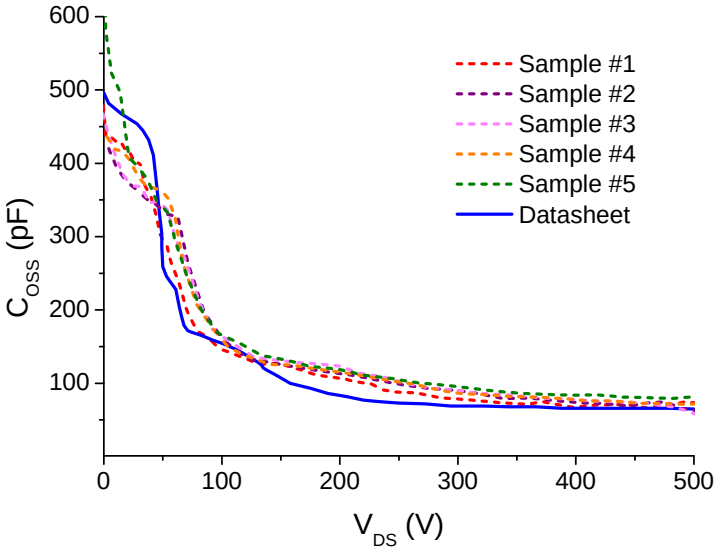


Figure 2.12: Output capacitances

trary to the integration of datasheet waveform, extracted energies of the samples have a good match with the reported value.

$$E_{OSS}(V) = \int_0^{V_{DS}} V C_{OSS}(V) dV \tag{2.12}$$

Experimental results show that this method is a fast and easy way to characterize the output capacitance. Nonmandatory high voltage power supply and reference capacitance selection are advantages of this technique. Moreover, it is possible to detect if the transistor experiences the same capacitance during charging and discharging. Even though the charging and discharging curves are symmetrical for GS66508T, some transistors have asymmetric voltage curves which cause another loss mechanism as reported in [16]. That asymmetry cannot be revealed by the Sawyer-Tower method.

In summary, this chapter focuses on the characterization of gate charge and output capacitance. In the first part, gate loss is characterized by three different methods and compared with each other. The results show that the datasheet provided gate charge is only valid for the hard-switching case and deviates from the actual value with 25% error. In the second part, the output capacitance and the stored energy

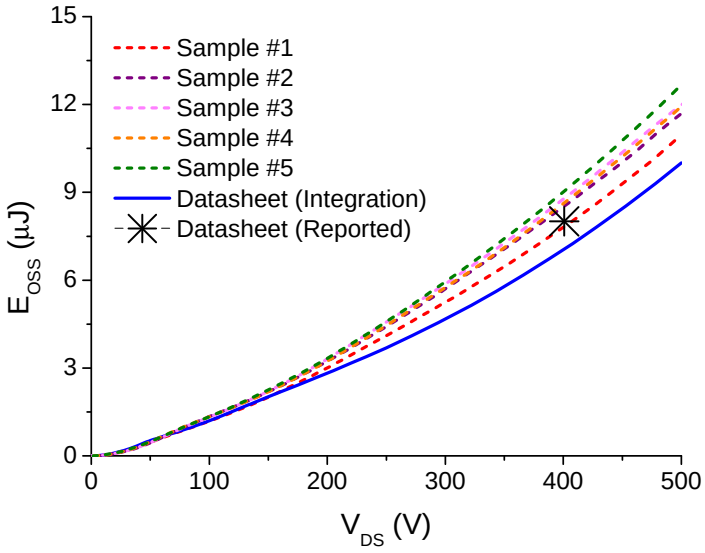


Figure 2.13: Stored energy on the output capacitance

of the GaN HEMT transistor are characterized by using a method proposed in the literature. Though the minor differences, the method gives a compatible result with the datasheet. The characterized output capacitance will be used for determining the dead-time period in Chapter 5.

CHAPTER 3

SWITCHING CHARACTERISTICS

Investigation of switching behavior of Gallium Nitride (GaN) power Field Effect Transistors (FETs) is important for several reasons. Initially, the sharp change in di/dt and dv/dt of GaN HEMTs make them susceptible to parasitic components. Secondly, e-mode GaNs are able to conduct in the reverse direction without an intrinsic body diode [17]. Though their resistive behavior in forward conduction mode like MOSFETs, they act differently in reverse conduction mode since the source-drain voltage depends on the gate-source bias level. As a result, both turn-on and turn-off characteristics are dependent on applied gate-source voltage. In order to inhibit an unintended turn-on during dead time, a negative gate bias is applied in half-bridges [9] which causes much higher dead-time losses. Moreover, studying the switching characteristics of GaN HEMTs is also important to understand the loss model separately for forward and reverse conduction modes because they are not the same as in Si MOSFETs. While estimating the switch losses, the dead-time period and power dissipation in that period could be ignored for Si MOSFETs but this may have a significant effect on the efficiency of e-mode GaN applications [9].

Switching characteristics of GaN HEMTs depend on several factors such as layout inductance on the gate loop (L_g) and the power loop (L_p), operating DC voltage (V_{DC}) because it changes the output capacitance (C_{oss}), junction temperature (T_j), in-package inductances of transistor (L_{sin}, L_{din}), applied gate voltage levels (V_{ON}, V_{OFF}) and turn-on & turn-off resistances (R_{on}, R_{off}).

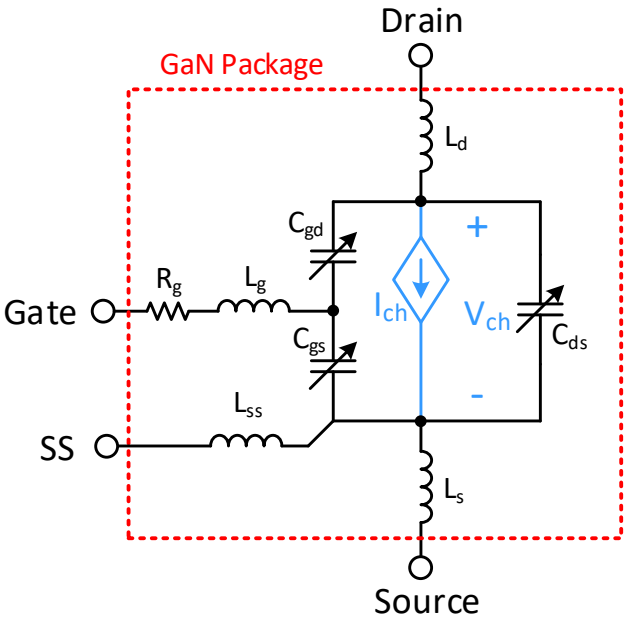


Figure 3.1: GaN Package Model [8]

3.1 Modelling GaN HEMTs

In this study, a hybrid model is proposed as shown in Fig. 3.1. In this model, the channel characteristic is modeled by a dependent current source, which varies with gate-source voltage, drain-source voltage, and temperature. The blue branch in Fig. 3.1 indicates the device channel where its current and voltage equals to I_{ds} and V_{ds} in steady-state, respectively. The analysis during the switching transients will be located onto these steady-state characteristics to show the regions that device operates during these transient periods as presented in Section 3.2. Moreover, the Kelvin source pin (SS) is included in the model to analyze the switching behavior clearly. Since the I_{ds} current flows through the source pin and since GaN FETs are able to switch fast, which results in a high di/dt ratio, the gate-source voltage is distorted because of the source parasitic inductance, in other words, common source inductance [2]. Thus, using the Kelvin source pin increases the stability reducing channel to gate feedback.

The equations used for steady-state models are shown in (3.1) and (3.2) for forward conduction and reverse conduction modes, respectively. These equations correspond to the $I_{ds} - V_{ds}$ curves of the device and the dynamic R_{ds-on}, derived from the manufacturer's models. The logarithmic multiplier of the equations represents the trans-

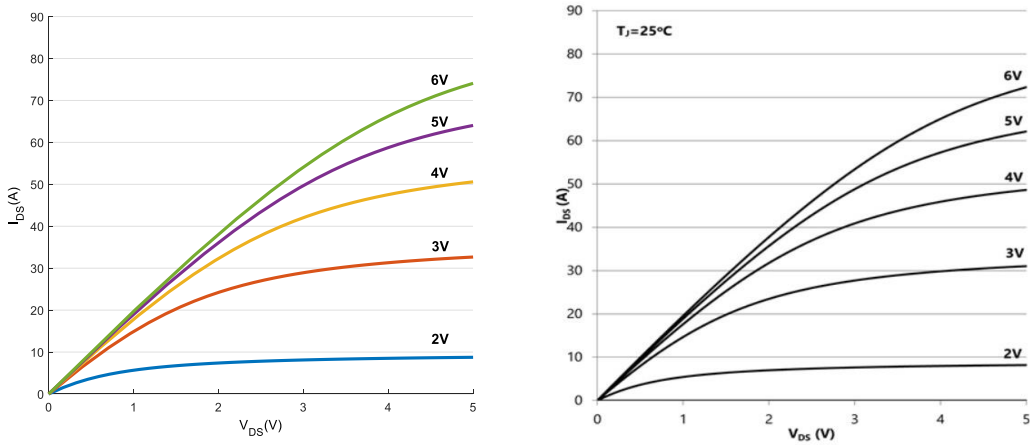
conductance of the device where V_{th} is the threshold voltage. The fractional multiplier represents the region in which the device is operating; i.e., active region or ohmic region. Using this model, both the steady-state and transient behavior of the channel is obtained.

$$I_{ds} = K_1(T)\ln(1 + e^{\frac{V_{gs}-V_{th}}{K_2}})\frac{V_{ds}}{1 + \max(K_4 + K_5(V_{gs} + K_9), K_7)V_{ds}} \tag{3.1}$$

$$I_{ds} = -K_1(T)\ln(1 + e^{\frac{V_{gd}-V_{th}}{K_8}})\frac{V_{sd}}{1 + \max(K_4 + K_5(V_{gd} + K_9), K_7)V_{sd}} \tag{3.2}$$

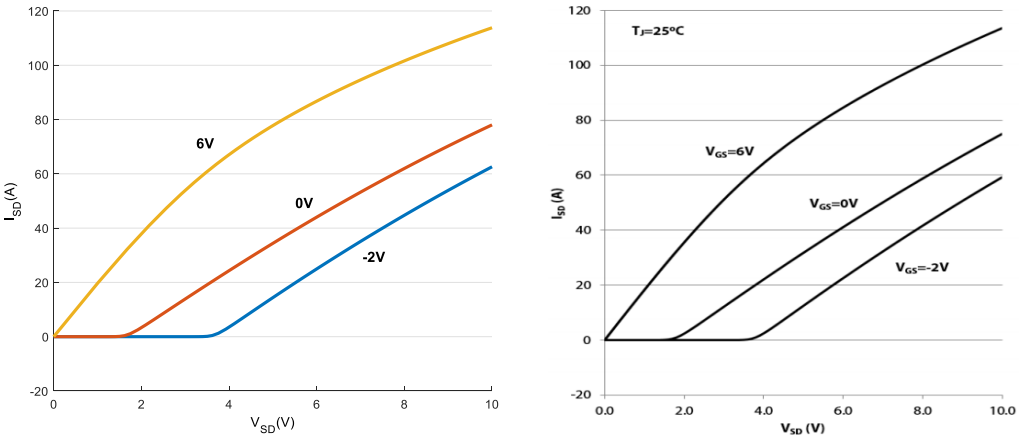
To show the accuracy of the steady-state models, I_{ds} vs V_{ds} characteristics of the selected device (GS66508T from GaN Systems) with varying V_{gs} voltage is obtained in both forward and reverse conduction regions at 25°C, and plotted side-by-side with the actual characteristics given in the datasheet of the selected device [5] in Fig. 3.2 and in Fig. 3.3 [8]. As shown in the figures, the reverse conduction behavior is highly dependent on the applied gate voltage and shows a different behavior at negative gate voltage. In freewheeling modes, this should make no difference since the applied gate voltage is positive. However, during dead-time periods, a negative gate voltage increases the reverse conduction loss, which makes the optimization of the negative gate voltage and dead-time duration very critical for high-frequency applications.

Secondly, the steady-state behavior of the GaN FETs is dependent greatly on the temperature, so its performance is affected by the temperature significantly as given in Fig. 3.4. The trans-conductance of the GaN transistor is nearly halved for every 75°C increase in junction temperature. Therefore, thermal analysis is required to investigate the switching behavior more precisely.



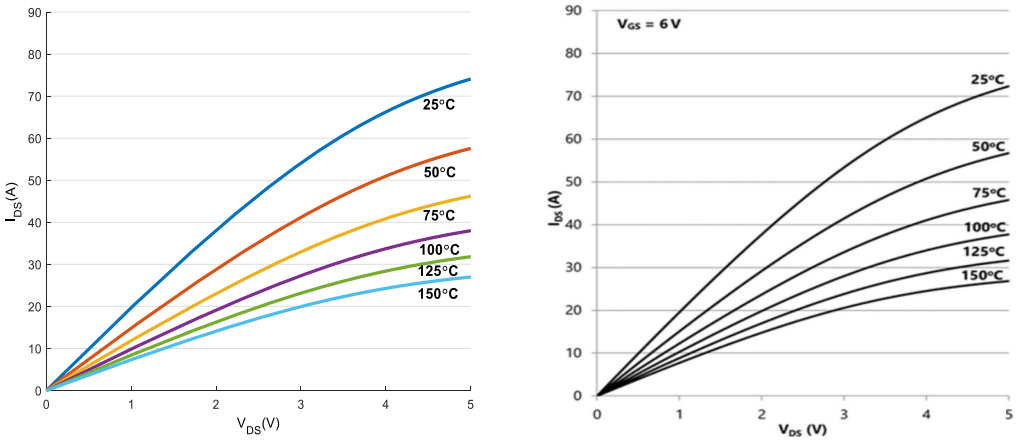
(a) Analytical Model (b) Manufacturer Datasheet [5]

Figure 3.2: Forward conduction characteristics for different V_{gs} voltages at 25°C of junction temperature [8]



(a) Analytical Model (b) Manufacturer Datasheet [5]

Figure 3.3: Reverse conduction characteristics for different V_{gs} voltages at 25°C of junction temperature [8]



(a) Analytical Model

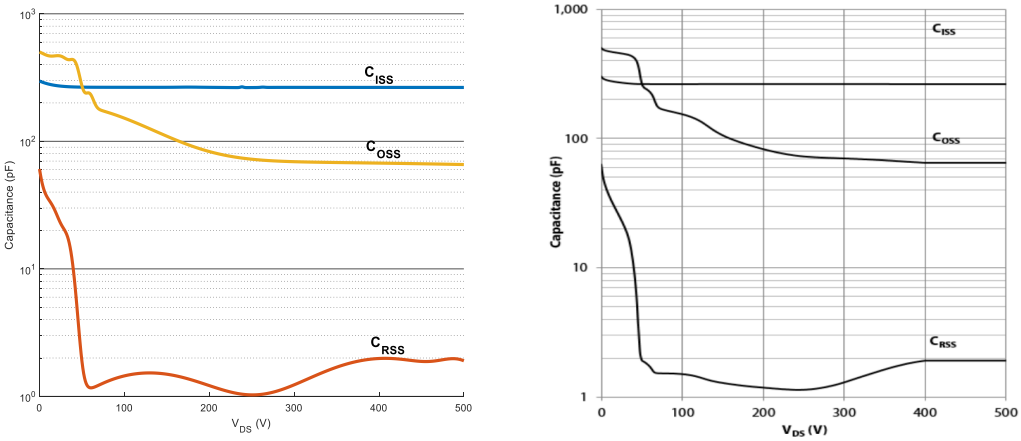
(b) Manufacturer Datasheet [5]

Figure 3.4: Forward conduction characteristics for different junction temperatures at 6V of V_{gs} voltage [8]

Thirdly, the voltage-dependent parasitic capacitances are modeled using curve fitting obtained from datasheet [5] and [9]. The resultant curves are given in Fig. 3.5 and Fig. 3.6. The manufacturer provides the curve for parasitic capacitances with respect to the drain-source voltage and it is seen that C_{ISS} is constant over V_{DS} voltage. However, the C_{ISS} changes significantly with varying gate-source voltage, and the model should be constructed by identifying the gate charge. Therefore, in order to model the dynamic behavior accurately, C_{ISS} vs V_{gs} curve is obtained from the reference graph given in [9].

3.2 Switching Behavior of GaN HEMTs

For a better understanding of the switching behavior of enhancement mode GaNs, the turn-on and turn-off behavior of the selected device is investigated with a DPT circuit as shown in Fig. 3.7 on MATLAB / Simulink platform. The switching behavior of e-mode GaNs are studied step-by-step using three models: the simplest model with constant capacitances and without parasitic inductances, the model with variable capacitances but without parasitic inductances, the most comprehensive model with variable capacitances and with parasitic inductances.



(a) Analytical Model

(b) Manufacturer Datasheet [5]

Figure 3.5: Package capacitances over V_{DS} voltage [8]

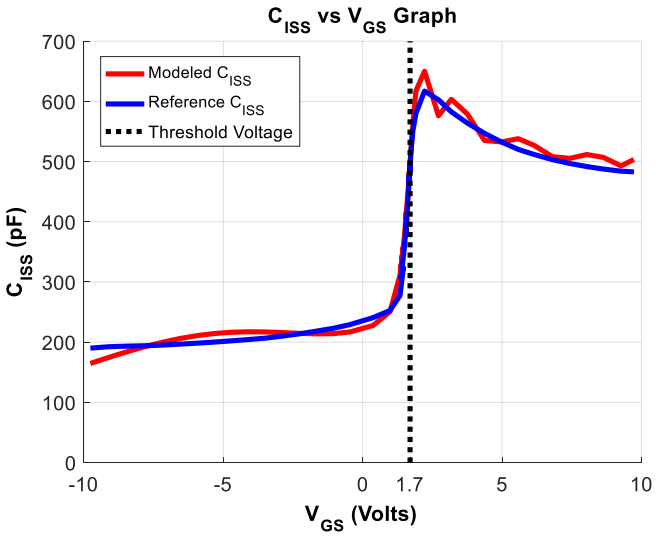


Figure 3.6: Input capacitance over V_{gs} voltage [8]

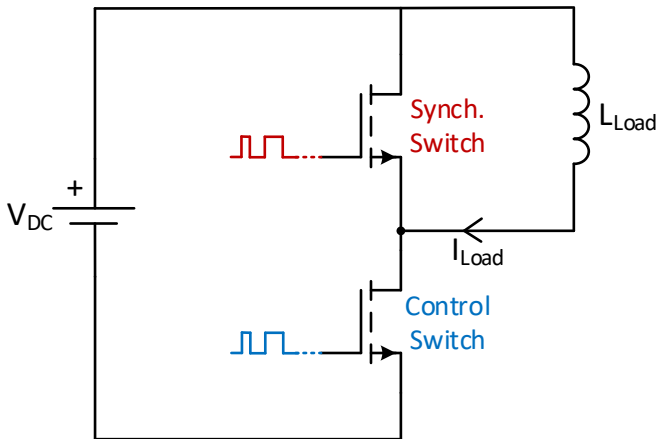


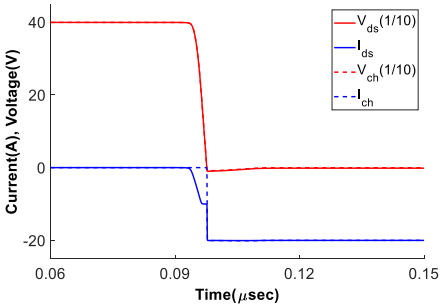
Figure 3.7: Double Pulse Test (DPT) circuit [8]

The further simulation results are given for the ratings shown in Table 3.1. These ratings are selected so that comparable results with datasheet could be obtained.

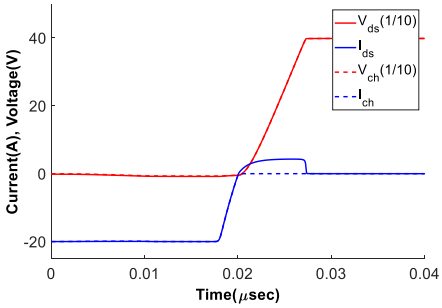
3.2.1 Model 1: The simplest model with constant capacitances and without parasitic inductances

For simplicity, the control switch is going to be labeled as "Bottom Switch" and the synchronous switch is going to be labeled as "Top Switch" from now on, in the DPT circuit. For Model 1 described above, turn-on and turn-off characteristics of the top and bottom switches are obtained against time and can be seen in Fig. 3.8.

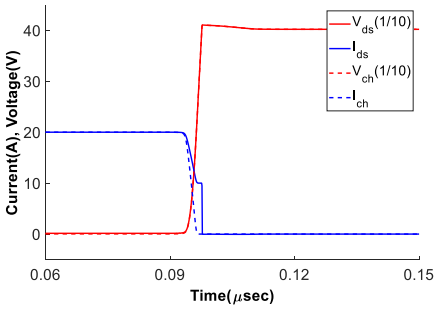
The drain-source current and the channel current is plotted together to clearly show the device characteristics. Since the inductances are not included in this model, the channel voltage is equal to the drain-source voltage in either steady-state or transient. However, since the capacitors are charged or discharged in transient periods, the channel current is different from the drain-source current and drain-source current does not reflect the channel characteristics completely. As shown in Model 1, Fig. 3.8(d), when the bottom switch is being turned on, the drain-source current and channel current make an overshoot with different amplitudes. Since the top switch stops conducting, $C_{OSS}(= C_{gd} + C_{ds})$ of the top switch requires to be charged which results in a positive current flow through the top switch. When the drain-source voltage of the top switch increases, the drain-source voltage of the bottom switch decreases, so



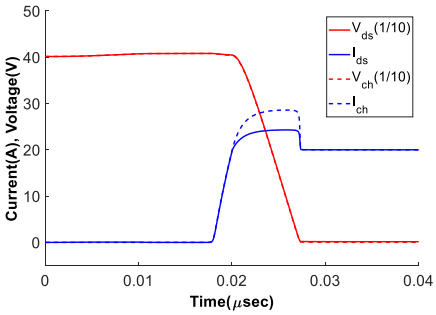
(a) Top switch turn-on



(b) Top switch turn-off



(c) Bottom switch turn-off



(d) Bottom switch turn-on

Figure 3.8: Switching transients obtained using Model 1 [8]

Table 3.1: Simulation parameters for switching characteristics

Operating voltage (V_{DC})	400 V
Internal gate resistance (R_{gin})	1.5 Ω
Load current (I_{Load})	20 A
Internal Drain Inductance (L_{din})	0.9 nH
Internal Source Inductance (L_{sin})	0.9 nH
Gate loop inductance (L_{gin})	3.0 nH
Power Loop Inductance (L_p)	7 nH
Turn-on gate resistance (R_{on})	10 Ω
Turn-off gate resistance (R_{off})	1 Ω
On-state gate voltage (V_{ON})	6 V
Off-state gate voltage (V_{OFF})	-3 V
Junction temperature (T_j)	$125°C$
Dead time (t_{dead})	20 ns

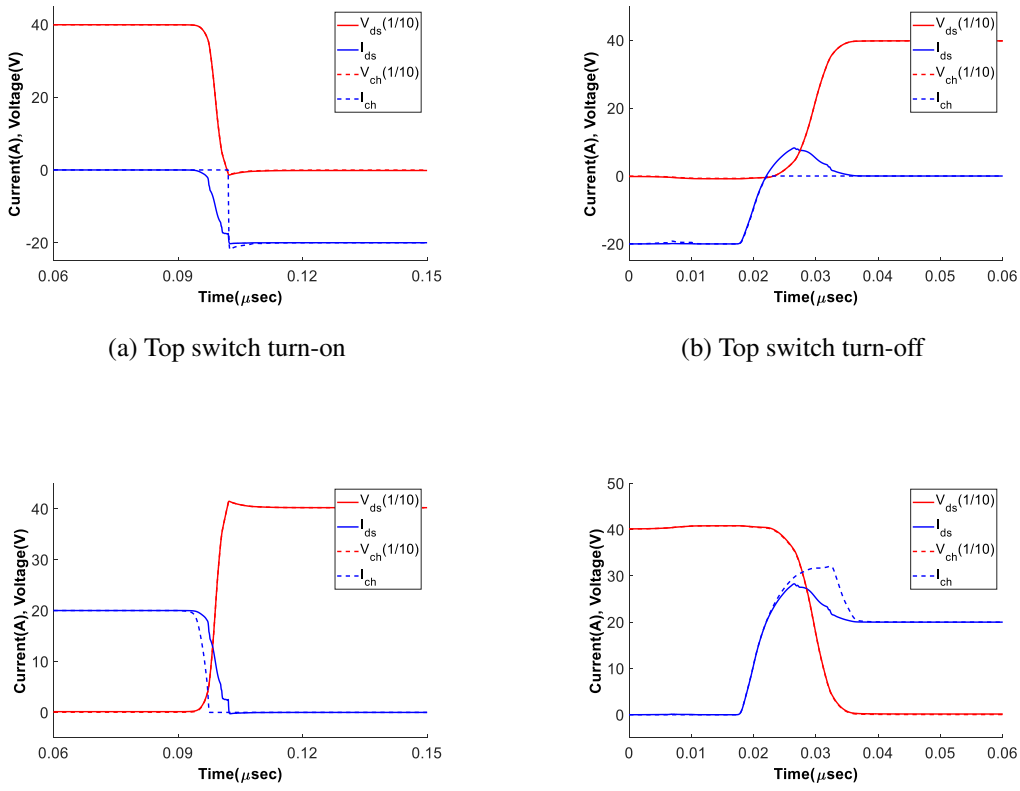
the C_{OSS} of the bottom switch discharges, which results in an extra overshoot in the channel of the bottom switch. Thus, even though the channel of the bottom switch is activated to discharge the C_{OSS} of the bottom switch, only the top switch effect on the drain-source current is observed. One should note that the main characteristics observed in Model 1 are important to understand GaN behavior because even though these characteristics exist in complicated models, it might be hard to catch them with the presence of oscillations due to parasitic inductances and varying capacitances.

3.2.2 Model 2: The model with variable capacitances but without parasitic inductances

In this step, the capacitance values, which were kept constant previously, are treated as variable capacitances using the capacitance models presented in the modeling section. As shown in Figure 3.5 and 3.6, the capacitances change with respect to the applied drain-source voltage and gate-source voltage. The turn-on and turn-off characteristics of the top and the bottom switches are obtained against time and can be

seen in Fig. 3.9.

In Model 2, again the drain-source voltage is directly equal to the channel voltage as expected. However, in this case, it is observed that the peak of the overshoot in the channel current and drain-source current of bottom switch increased because C_{OSS} is greater for lower drain-source voltages, which results in higher current flow under similar voltage change in time. Therefore, in order to estimate the overshoot amplitude correctly, the parasitic capacitances should be modeled properly. Moreover, for all transient periods given in Figure 3.9, it is observed that the voltage changes are smoother, which makes the model more realistic.



(a) Top switch turn-on

(b) Top switch turn-off

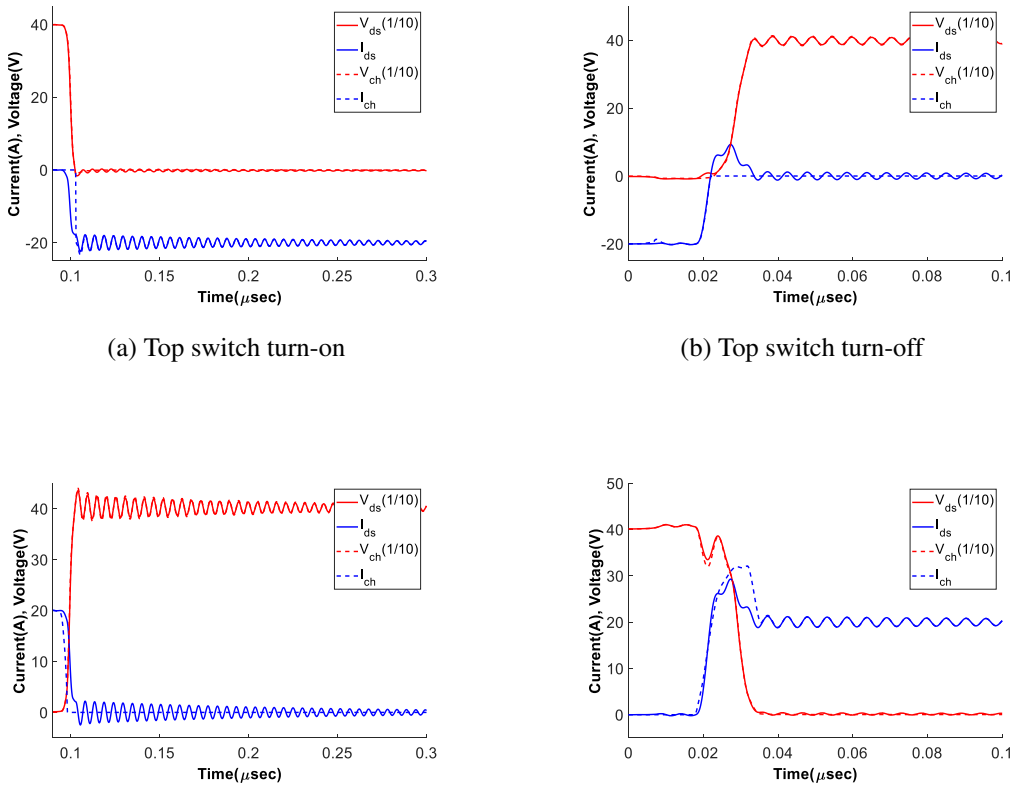
(c) Bottom switch turn-off

(d) Bottom switch turn-on

Figure 3.9: Switching transients obtained using Model 2 [8]

3.2.3 Model 3: The most comprehensive model with variable capacitances and with parasitic inductances

Finally, to see the effect of the oscillations created by the LC resonance paths, the parasitic inductances are added to the model, which are caused by packaging, bus bar, conducting parts on the DC side and Capacitor ESLs. In Model 3, in which all the parasitic effects are included, as shown in Fig. 3.10, the oscillations started to emerge due to energy transfer between parasitic capacitances and inductors. In addition, a large dip is observed during the turn-on transient of the bottom switch due to the voltage induced on the power loop inductance by the switching current. Even though loop inductance is not related to the transistor type, due to the fast switching capability of GaN FETs, the voltage drop increases relatively in comparison to other types of semiconductors. Moreover, in Fig. 3.10, it is observed the oscillation damps



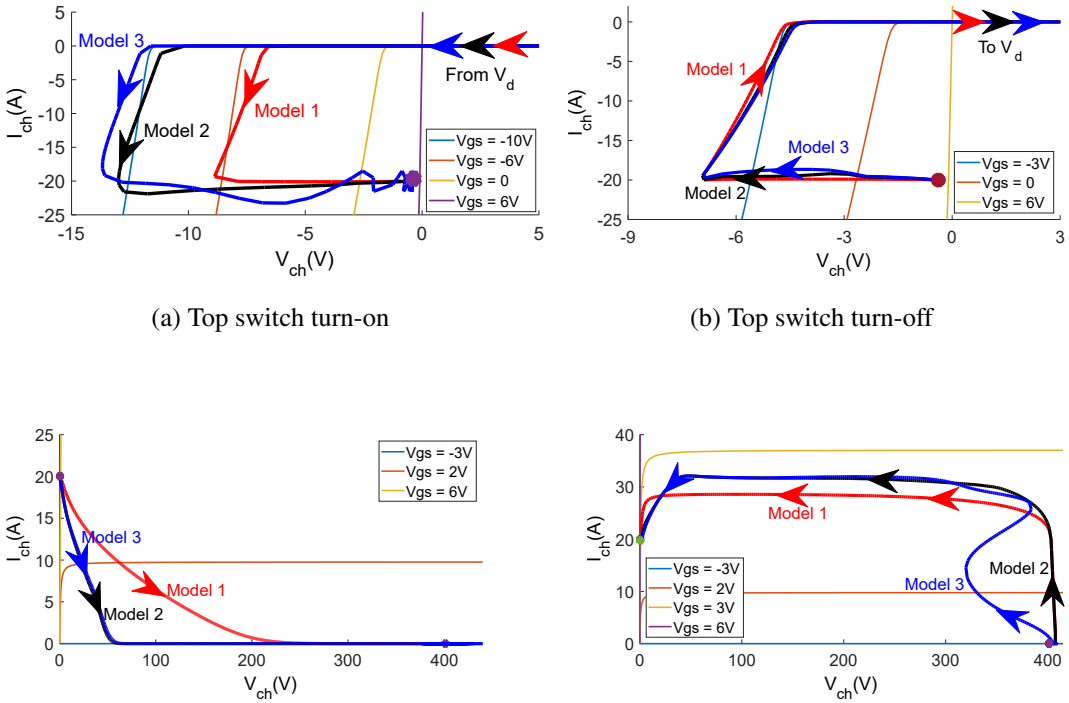
(a) Top switch turn-on

(b) Top switch turn-off

(c) Bottom switch turn-off

(d) Bottom switch turn-on

Figure 3.10: Switching transients obtained using Model 3 [8]



(a) Top switch turn-on

(b) Top switch turn-off

(c) Bottom switch turn-off

(d) Bottom switch turn-on

Figure 3.11: State-trajectories obtained for different models [8]

in time. The damping duration of the oscillation is studied in [49] and it is shown that the damping duration is dependent on the C_{OSS}, loop inductance, and drain/-source parasitic inductances and trans-conductance. Since the increasing temperature reduces the trans-conductance, the oscillation damps faster as junction temperature gets higher as stated in [49].

3.2.4 State Trajectories

In order to show these transients better, the I_{ch}, V_{ch} paths, which the top and the bottom switches follow during turn-on and turn-off periods, are also obtained as state trajectories and given in Fig. 3.11, in Fig. 3.12, in Fig. 3.13. These trajectories are plotted on the device steady state current-voltage characteristic as given in Fig. 3.2 and in Fig. 3.3.

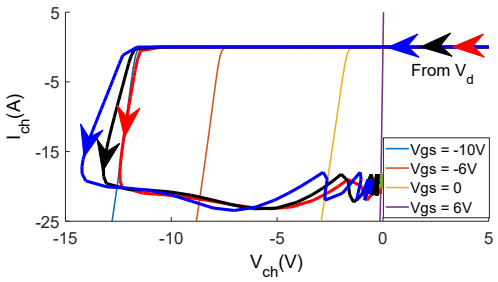
When we look at the trajectory for the turn-on period of the Bottom Switch, Fig. 3.11(d), it is easy to see the Miller Plateau where the voltage drops and current stays

constant ideally. The importance of using the Kelvin source pin can be deduced here. When the current changes, a voltage is created on the source parasitic inductance as described earlier. Therefore, if the Kelvin Source pin is not used, huge vertical oscillations would be observed on the state-trajectories due to the oscillations on gate-source voltage. However, now the channel seems very stable though the high di/dt ratio of the channel. Moreover, it is observed that the main channel behavior is in two directions; that is, in general, the channel state moves either horizontally or vertically. The horizontal movement of the channel state for the first quadrant, i.e. forward conduction, means the channel voltage changes while the gate-source voltage and channel current stay constant. However, vertical movement of the channel state in the first quadrant means the channel current and gate-source voltage varies while channel voltage stays constant. On the other hand, for the third quadrant, i.e. reverse conduction, when the channel state moves horizontally, the channel voltage and gate-source voltage change while the channel current does not vary. Conversely, vertical movement of the channel state means the channel current varies while the channel voltage and gate-source voltage stay constant. The third quadrant behavior of the GaN FETs is unique because the channel is able to conduct in the reverse direction with any gate-source voltage.

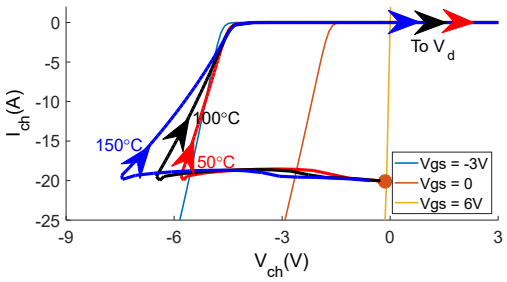
Furthermore, focusing on the trajectories given in Fig. 3.11(a), the channel state moves first vertically and then horizontally after conduction starts in channel. The conduction starts because the Bottom Switch is being turned off and dead time begins. Therefore, the channel is activated even though the gate-source The voltage of the Top Switch is not changed yet. Then, changing the gate-source voltage from -3V to 6V do not affect the channel current but it only decreases the reverse conduction losses. In order to simplify the concept, the rise of the channel current can be called as **active turn-on** and increasing the gate-source voltage can be called as **passive turn-on** because it changes nothing for channel current but only decreases the losses. Similarly, in Fig. 3.11(b), the channel state first moves in horizontal direction and then it moves vertically before the current falls to zero. Due to the safety considerations, before firing the bottom switch, the top switch gate-source voltage should be decreased; however, the channel current of the top switch is not affected by the change in gate-source voltage. The channel current falls to zero when the bottom

switch is fired and it starts conducting. Therefore, reducing the gate-source voltage can be called as **passive turn-off** and the fall in the current can be called as **active turn-off**. Even though this unique behavior of the GaN FETs is discussed in the literature, having these definitions make the concept more understandable. In IGBTs or MOSFETs, current flows through the anti-parallel diode or body diode, respectively, during the reverse conduction. Therefore, the channel is not turned on or off. However, in GaN HEMTs, since body diode or anti-parallel diode does not exist, the reverse current flows through the device channel always.

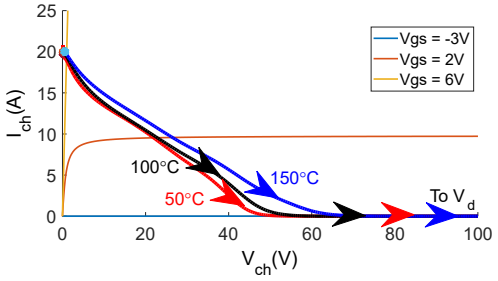
In Fig. 3.12, the channel state trajectories are given for Model 3 at different junction temperatures. It is observed in (a), (b) and (c), the channel voltage and gate-source voltage are high in amplitude during transition at high junction temperatures due to the low trans-conductance. In Fig. 3.12(d), it is seen that the temperature increases the stability and reduces the current rise and voltage fall speed. A horizontal dip is observed due to the voltage created on the loop inductance when the current rises



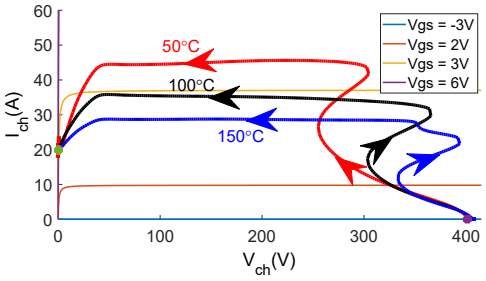
(a) Top switch turn-on



(b) Top switch turn-off



(c) Bottom switch turn-off

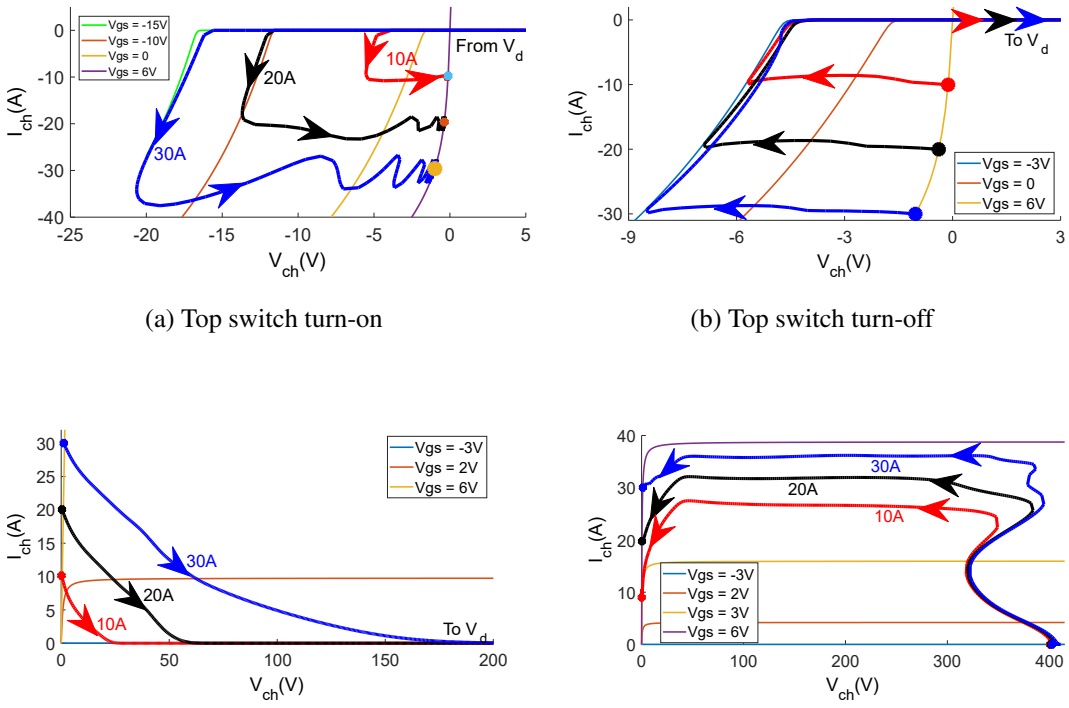


(d) Bottom switch turn-on

Figure 3.12: State-trajectories obtained for different junction temperatures using Model 3 [8]

immediately. However, for the higher junction temperatures, the decrease in the voltage is small because of the reduced switching speed of the GaN FET. Similarly, for the rest of the transition, the channel current makes the maximum overshoot for the lowest junction temperature as expected for the same reason.

In Fig. 3.13, it is observed that the gate-source voltage is significantly affected by the channel current during the transition. In (a), it is seen that the gate-source voltage decreases dramatically in transient period for high channel current because when the load current commutes from the bottom switch to top switch the load current discharges the gate-source capacitance instantaneously so as to reach the right conduction state before the gate-source voltage is set to high. In addition, as shown in (d), the channel voltage drops equally for all current ratings as expected because the load current does not change the GaN FETs transition speed.



(a) Top switch turn-on

(b) Top switch turn-off

(c) Bottom switch turn-off

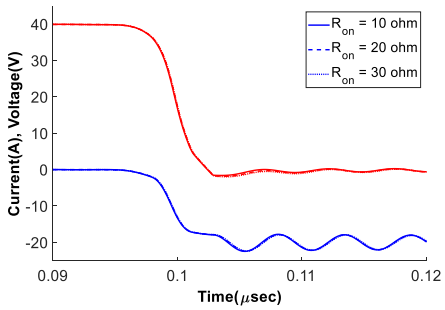
(d) Bottom switch turn-on

Figure 3.13: State-trajectories obtained for different load currents using Model 3 [8]

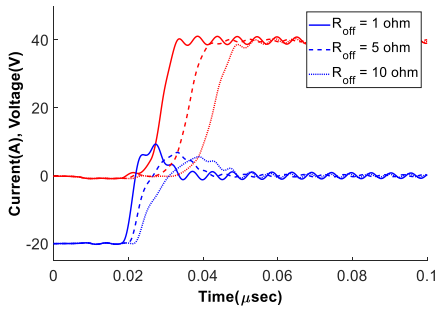
3.2.5 Effect of Gate Resistances

Lastly, the effect of the turn-on and turn-off resistances are investigated as given in Fig. 3.14. The turn-on and turn-off speed of the GaN FET is related to how fast the gate-source capacitance is being charged or discharged. With low gate driver resistances, the gate-source voltage changes rapidly. Therefore, as resistances get higher, the switching speed decreases, so the transition takes longer. However, this is only valid for active turn-on or active turn-off as presented in (b) and (d). Contrary to these cases, gate resistances do not affect the transient speed for the passive turn-on and the passive turn-off as shown in Fig. 3.14 (a) and (c). It only affects the delay time for the gate-source voltage to reach the Miller Plateau level as shown in (c). Additionally, due to the reduced switching speed, the voltage drop caused by the loop inductance decreases for high gate driver resistances but the switching losses are increased as well.

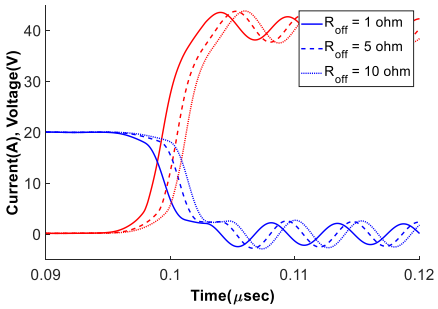
To sum up, switching behavior of GaN HEMTs depends both on device parameters and circuit parameters. Junction temperature is an important parameter slowing down the transient speed and increasing the on-state resistance. Moreover, in a proper model of the transistor, variable parasitic capacitance has to be included for accuracy. For maximizing accuracy and observing the effects of circuit parameters, inductance models are also required to be added. Additionally, key terms regarding turn-on and turn-off are defined in this chapter. An active turn-on and turn-off define the change in gate state prior to switching transient of the device channel. Similarly, passive turn-on and turn-off mean the transient on the channel happens before gate state change.



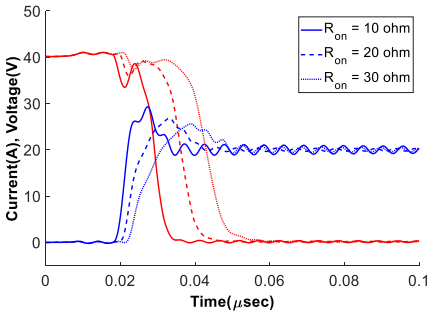
(a) Top switch turn-on



(b) Top switch turn-off[8]



(c) Bottom switch turn-off



(d) Bottom switch turn-on[8]

Figure 3.14: Effect of gate resistances on transient behavior

CHAPTER 4

SHORT-CIRCUIT PROTECTED HALF-BRIDGE DESIGN AND LAYOUT OPTIMIZATION FOR GAN HEMT TRANSISTORS

A generic half-bridge consists of two transistors, their gate driver circuits, and bypass capacitors for filtering high-frequency oscillations. In this chapter, a half-bridge board design that can be used for different applications is proposed. The proposed half-bridge board consists of two paralleled half-bridges, their gate driver circuits including a gate driver integrated circuit (IC), and an isolated converter IC, an ultra-fast shoot-through type short circuit protection mechanism as presented in Fig. 4.1. A three-dimensional view of this design can be seen in Fig. 4.2.

A half-bridge design includes several critical steps such as optimized layout design for both the power loop & the gate loop and thermal design. On top of these points, layout considerations for parallel-connected transistors and short circuit protection are also investigated in this chapter.

4.1 Layout Design

Most of the common converters include at least one half-bridge for regulating output voltage and current. Switch-mode power supplies and voltage source inverters are examples for those converters. The output ratings are regulated by switching transistors with a PWM signal. Switching a transistor means changing the path of the current either by starting flow or stopping it in a short amount of time. This sharp rise or fall in current makes circuit sensitive for layout parasitics, especially for layout inductances. Considering the faster switching capability of GaN HEMTs with respect to other types of transistors, layout optimization is a must for safe operation.

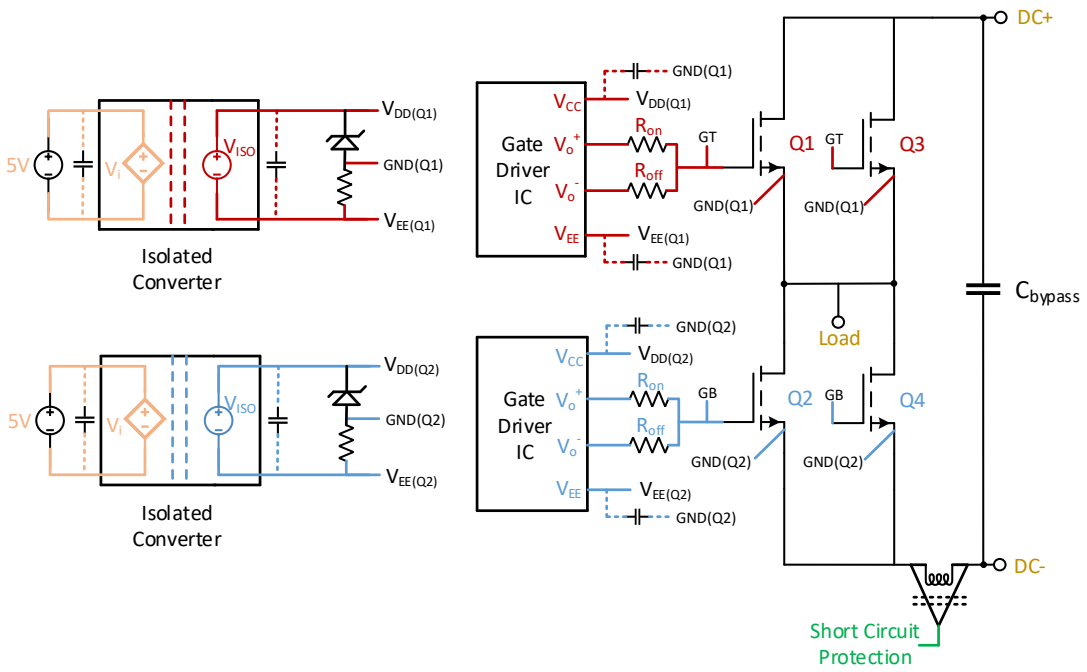


Figure 4.1: Circuit schematic of proposed half-bridge design

Layout inductances should be minimized for the power loop and the gate loop as will be discussed in the following sections. For parallel-connected transistors, not only inductance minimization is required but also distributing inductance as even among parallel-connected transistors is required for guaranteeing simultaneous switching. For analyzing layout parasitics, ANSYS Q3D Extractor and ANSYS Maxwell 3D finite element analysis (FEA) tools are used.

4.1.1 Power Loop Design

The power loop is a critical current path in which both of the transistors play a role during the switching. An illustration of the power loop is given in Fig. 4.3. As seen on that figure, the inductive load is charged when Q2 is ON and, it free-wheels on Q1 when Q2 is OFF. At the moment when Q2 is being turned-off, the load current commutates from Q2 to Q1 reducing the amount of current on i.e. power loop inductance (L_p). L_p is an equivalent value of all the inductances distributed on the power loop. The decreasing current on L_p induces a negative voltage on the power loop inductance and since Q1 is being turned-on, drain to source voltage on Q2 rises up to

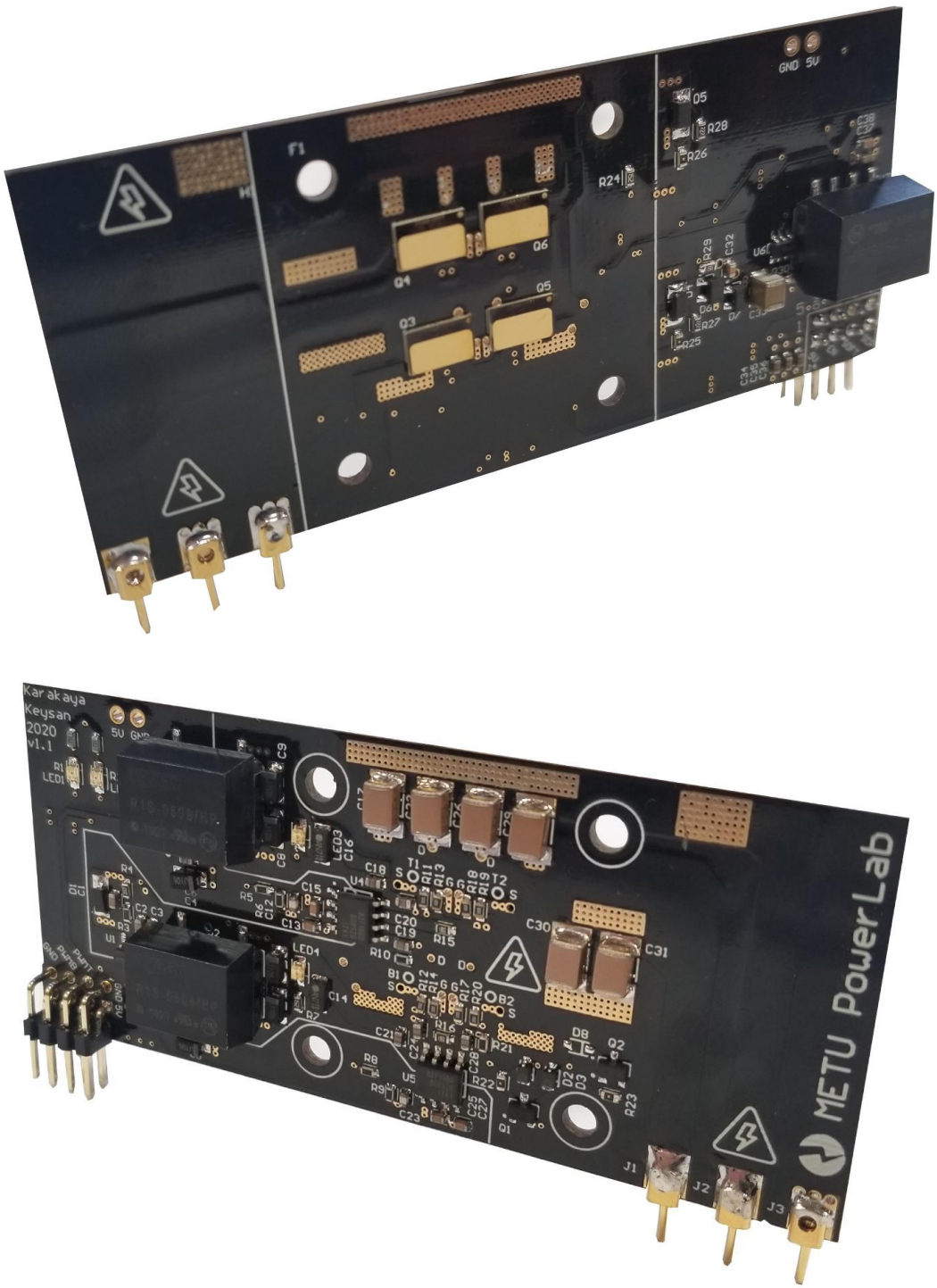


Figure 4.2: Three dimensional view of the half-bridge board

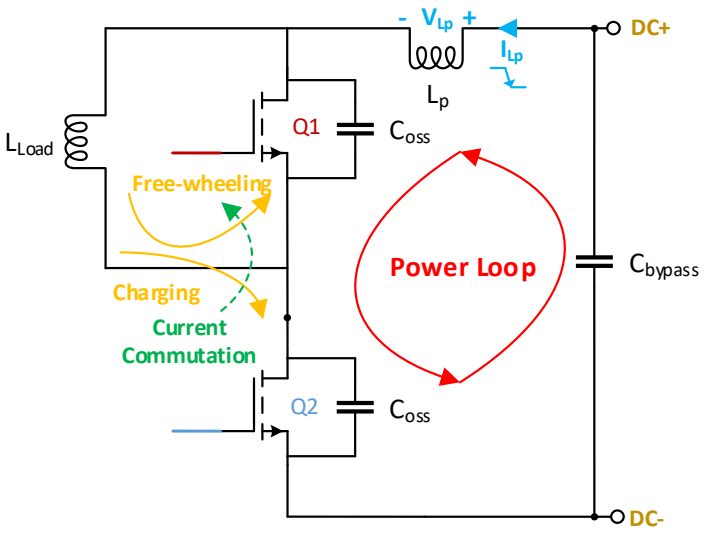


Figure 4.3: Definition of the power loop

a level higher than V_{DC} as given in (4.1). Therefore, Q2 must withstand not only with the DC link voltage but also additional induced voltage as well. Therefore, power loop inductance plays a significant role in stresses over transistors. Especially for GaN HEMTs, a non-optimized power loop design could lead to failure of operation easily because of the current transition speed of GaN HEMTs extend up to 10 A/ns.

$$V_{DS(Q2)} = V_{DC} - L_p \frac{dI_{L_p}}{dt} \tag{4.1}$$

After an overshoot, drain-to-source voltage comes to a steady-state level, i.e. supply voltage. However, before reaching the steady-state, oscillations emerge on $V_{DS(Q2)}$ at the resonance frequency as described in (4.2). Considering the relatively low level of output capacitance (~200-300 pF) and power loop inductance(~0.5-3 nH), oscillations frequency is around 100 - 400 MHz. This high frequency of oscillation and sharp rise or fall in power loop current should be counterbalanced with a high-frequency bypass capacitor. As shown in Fig. 4.3, bypass capacitors are also a member of the power loop and it should be placed close enough to manage oscillations. The Self-impedance of the bypass capacitor is also critical. Ceramic capacitors are preferred due to low impedance at the oscillation frequency range. Multiple numbers of bypass capacitors

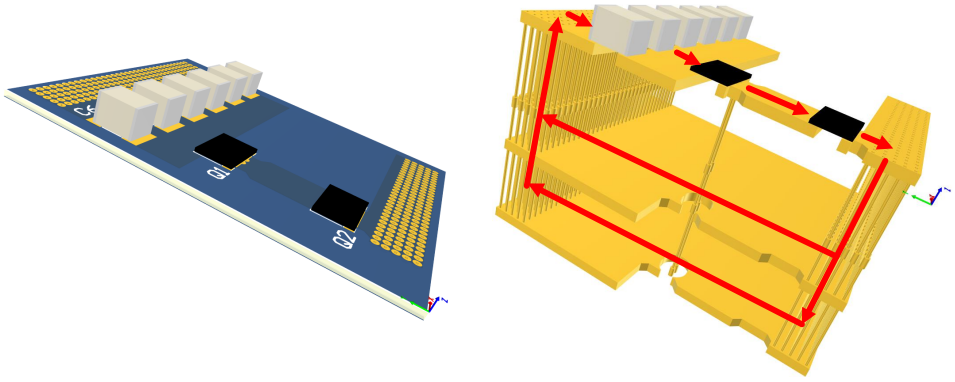
should be connected to obtain a low impedance.

$$f_{osc} = \frac{1}{2\pi\sqrt{L_p C_{OSS}}} \tag{4.2}$$

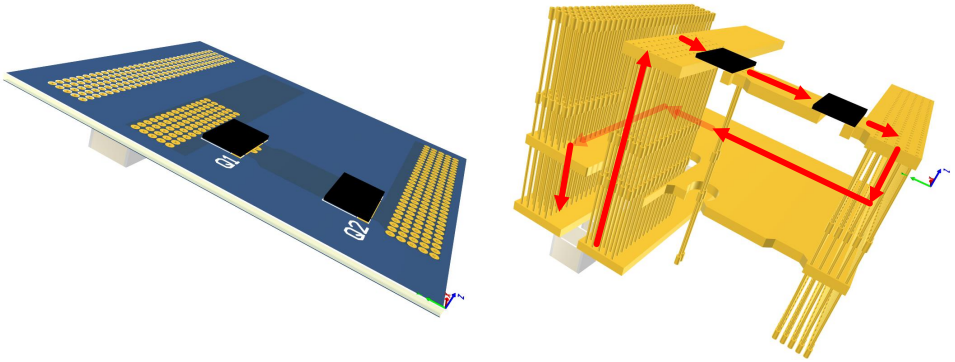
Since the placement of bypass capacitors affect the power loop inductance directly, their placement should be optimized to obtain minimum power loop inductance. For this purpose, a case study approach has been performed for a power loop inductance minimization of a half-bridge including two GaN HEMTs and six high-frequency bypass capacitors. For GaN HEMTs, GS66508T transistors are used from GaN Systems and C4532X7T2J224M200KC from TDK Corporation is used for bypass capacitors.

As presented in Fig. 4.4, there are three different designs in which the bypass capacitors are placed differently. Also in Fig. 4.4, current paths are illustrated for each design on a four-layer printed circuit board (PCB) design. In Design 1, bypass capacitors are placed on the same layer with GaN HEMTs, so they can be connected directly. The returning current path is placed just underneath the GaN HEMTs for minimizing the loop area. Design 2 is suggested by the transistor manufacturer [50] and the capacitors are placed on the bottom layer. It is aimed to separate the power loop into two closed small loops so that inductance can be minimized. Lastly, in Design 3, similar to Design 1 capacitors are kept on the same layer with GaN HEMTs but two of them are moved next to the transistors.

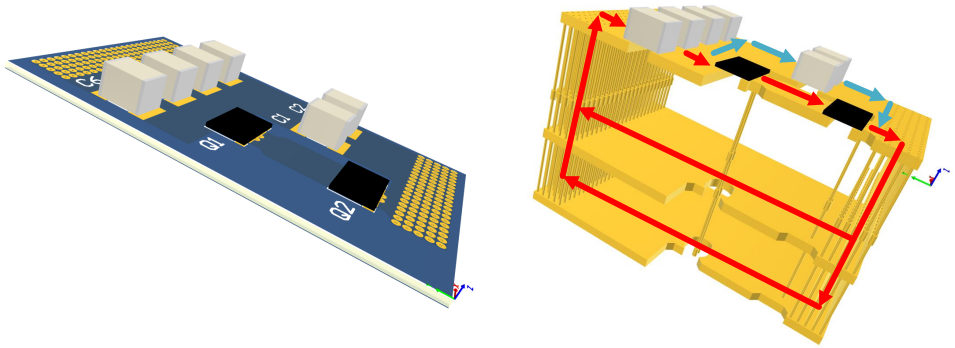
All configurations are investigated with ANSYS Q3D Extractor tool and the power loop inductance value is given for each design in Table 4.1. As expected Design 1 and Design 2 give close results around 5 nH. However, Design 3 has the lowest power loop inductance as 3 nH. It is a result of the maximum utilization of bypass capacitors. In the first two designs, the capacitors which are far away from the transistors cannot be utilized well enough due to high path impedance between those capacitors and transistors. In the last design, the farthest capacitors are placed close to half-bridge and they also contribute actively. As a result, effective layout inductance gets decreased.



(a) Design 1



(b) Design 2



(c) Design 3

Figure 4.4: Options for high-frequency bypass capacitor placement and power loop current paths for each design in exaggerated view

Table 4.1: Power loop inductance values for different designs

Design 1	5.00 nH
Design 2	5.06 nH
Design 3	2.98 nH

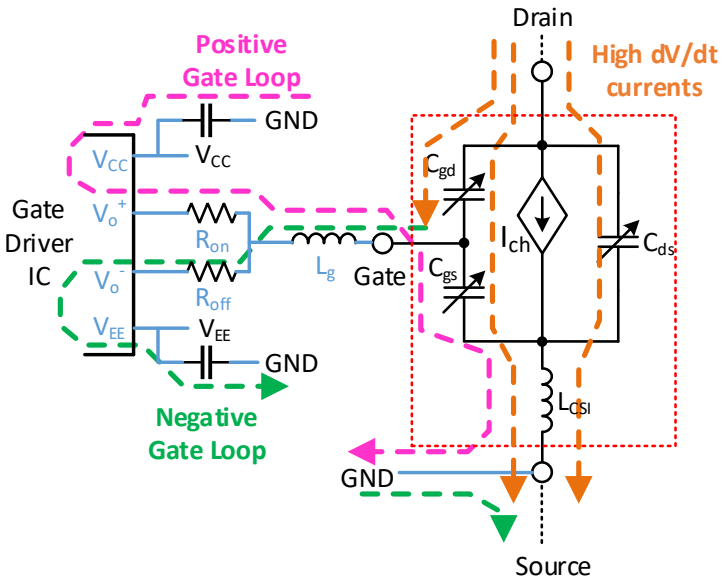


Figure 4.5: Definition of gate loops

4.1.2 Gate Loop Design

Similar to the power loop layout inductance, the gate loop layout inductance should be minimized to obtain the best switching performance. Whenever the gate driver IC changes its state, input capacitance of GaN HEMT ($C_{ISS} = C_{gs} + C_{gd}$) should be charged or discharged. Non-optimized layout design for the charging or discharging current path could increase the delay time for turn-on or turn-off. Moreover, high-frequency oscillations on gate-source terminals result in high-amplitude oscillations on channel current due to oscillating trans-conductance as discussed in detail in Chapter 3. This high oscillation on channel current radiates around the room which can couple with other digital or analog signals easily. Due to the high transition speed of GaN HEMTs, the frequency of this EMI noise is higher which increases the risk of system-level failure.

Furthermore, an optimization of the gate loop inductance is not only critical for the system but it is also critical for the safety of the transistor itself. As shown in Fig. 4.5, during a turn-off, output capacitance of transistor (C_{OSS}) is charged within a couple of nanoseconds. It is reported in [50], the charging speed could be as high as $60\ V/ns$ or $60\ kV/\mu s$. This fast transition leads to current flow through package capacitances of transistors. Here, the Miller Capacitance (C_{gd}) plays a significant role by constructing a feedback path from the power loop to the gate loop. The current coming through the Miller Capacitance can flow through either C_{gs} or negative gate loop as illustrated in Fig. 4.5. Ideally, the whole current should follow the negative gate loop path and it should not charge C_{gs} when C_{gs} is supposed to stay at a low state. However, due to the impedance of the path, some amount of current flows through C_{gs} and charges the capacitance. Since the other transistor on half-bridge is ON state at that moment, if the voltage on C_{gs} exceeds the threshold level, the channel gets activated which causes a short circuit failure. This failure is called a false turn-on in literature [9]. From now on, it is the question of how much impedance should a designer provide on the gate loop and the answer is as minimum as possible. Therefore, the gate driver should be placed close to GaN HEMTs, and high-frequency bypass capacitors should be connected to obtain a low impedance on the loop.

In the design of the gate loop layout, there are fewer actions to take in comparison to the power loop design. Because of the space limitations, it is not possible to place the multiple numbers of bypass capacitors or arrange their position for the best design. The actions are limited by placing gate resistances and bypass capacitors close to the transistor, using wide copper fields for carrying current and directing the loop current to return back to the source from the underneath of the incoming current. The optimum gate design can be obtained as long as these three rules-of-thumb are followed. The transistor manufacturer also recommends these actions [50] and the PCB view of this design can be seen in Fig. 4.6. For this design, the layout inductances are 0.88 nH and 0.93 nH for positive and negative gate loops, respectively.

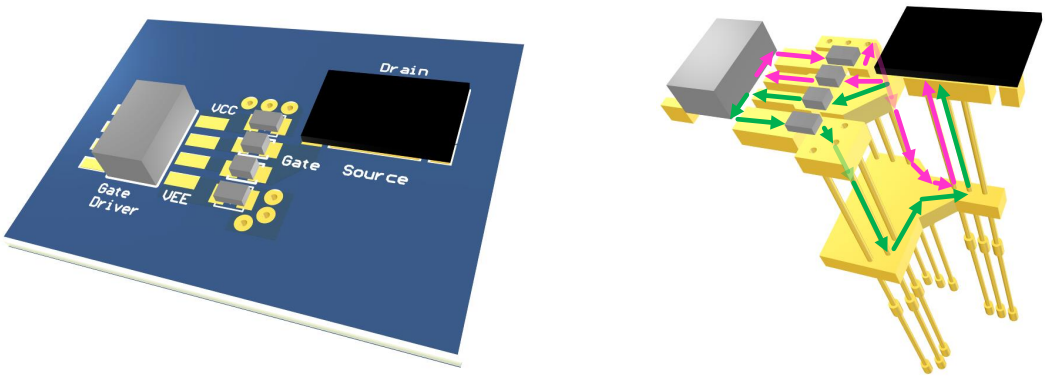


Figure 4.6: Printed circuit board design of gate loop and current paths for positive (pink) and negative (green) gate loops

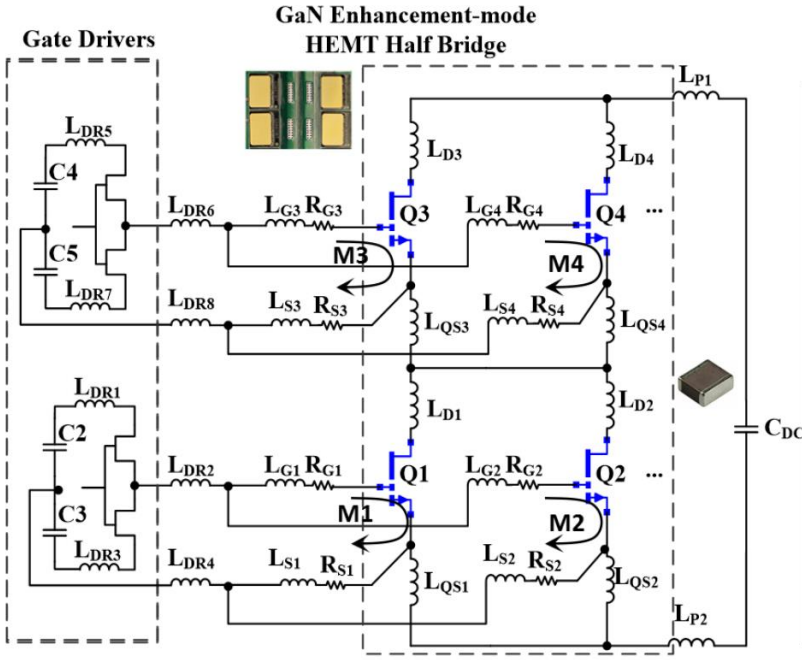


Figure 4.7: Parasitic inductances for parallel connected transistors operation [23]

Effects of Parasitics

Parameter	Description	Effect	Priority	Design Rules
L_{P1},L_{P2} $L_{D1\text{-}4}$	Commutation Loop Inductance	Increase Vds spike during P3 of Switching off	High	Smaller the better
L_{DR1}-L_{DR8}	Gate drive loop inductance	Increase Vgs ringing and overshoot	Medium	Smaller the better
L_{G1}-L_{G4} L_{s1}-L_{s4}		1. Increase Vgs ringing and overshoot, 2. susceptible to gate oscillation if very unbalanced	Medium	Smaller the better, as equal as possible for paralleled devices
M1-4	Mutual Inductance between power loop and gate loop	1.Feedback di/dt to Vgs, 2. Slowdown switching 3. potentially cause gate oscillation	Extremely High	
$L_{QS1\text{-}6}$	Quasi-common source inductance	1. Feedback the difference of di/dt to Vgs, 2. Balance current sharing 3. Potentially cause gate oscillation	Extremely High	

Figure 4.8: Effects of and design rules for parasitic inductances [23]

4.1.3 Design Optimization for Parallel Connected Transistors

Transistor paralleling is challenging because its hard to get the same losses on the parallel-connected transistor. However, it is possible if the semiconductor is suitable for paralleling. The transistor channel resistance should have a positive thermal coefficient (PTC) to get a natural balance. In the case of the uneven loss distribution, one of the transistors heats up much more resulting in increased channel resistance. Therefore, the current will start flow through the transistor with lower channel resistance and then it will heat up much more. Therefore, the transistors will get in a thermal balance in the final situation. Fortunately, GaN HEMTs are PTC type transistors as shown in Fig. 3.4. Thus, GaN HEMTs are naturally suitable for parallel operation with necessary layout design considerations.

Even though the same rules apply for the layout design of parallel-connected transistors, there are more restrictions such as distributing the layout inductance as even among parallel transistors. It is important to have a simultaneous switching transition between parallel devices. It is always assumed that the current is shared equally

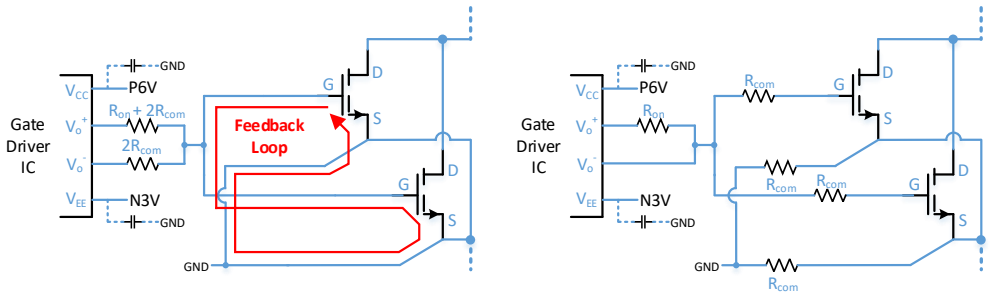
among parallel-connected transistors but it would not be the case if there is a difference in design. A mismatch can lead to increased switching loss on one of the transistors and it can lead to a thermal run away.

The design rules of parallel-connected transistors is well-studied in [23] and the inductance map and effect of parasitics are given in 4.7 and in 4.8, respectively. As shown in 4.8, commutation loop inductance; in other words, power loop inductance has a high priority and it should be kept small. Similarly, the gate loop inductances should also be kept small. However, it is not enough to keep the mutual coupling and quasi-common source inductances small. They also need to be equal for parallel-connected transistors. These two inductances show similar effect and they basically oppose the gate driver during the switching and slow down the transition. As a result, these inductances need to be distributed equally. Fortunately, it is not the only action a designer can take. Having separate gate resistors ($R_{G_{1-3}}$,$R_{G_{2-4}}$,$R_{S_{1-3}}$,$R_{S_{2-4}}$) for each transistor is critical to slow down or speed up the transition of any desired transistor. This also helps to compensate for in-package differences.

The designed half-bridge board is a result of the same design algorithm and its gate circuit is presented in Fig. 4.9. In 4.9(a), the gate resistors are placed such that gate and source terminals of transistors are directly connected. This configuration leads to feedback from one transistor to another one during the transient. In order to eliminate this feedback, the gate driver resistances can be distributed so that enough damping components can be obtained on the feedback loop. Moreover, distributed gate resistors enable to control the transition speed of each transistor separately. Actual values of R_{on} and R_{com} are 18 Ω and 1 Ω; therefore, turn-on resistance is 20 Ω and turn-off resistance is 2 Ω.

In the light of these layout considerations, two transistors are paralleled to increase current handling capability to 60 Ampẽres. Paralleling two GS66508T (650V/30A) transistors is more advantageous than using a single GS66516T (650V/60A) transistor because of the cost and thermal considerations. Having four different transistors increases the contact area of heat sink resulting in a better cooling performance as will be discussed in Section 4.3 in detail.

Layout analysis is performed on ANSYS Q3D for parallel-connected transistors in the



(a) Non-distributed gate resistances

(b) Distributed gate resistances

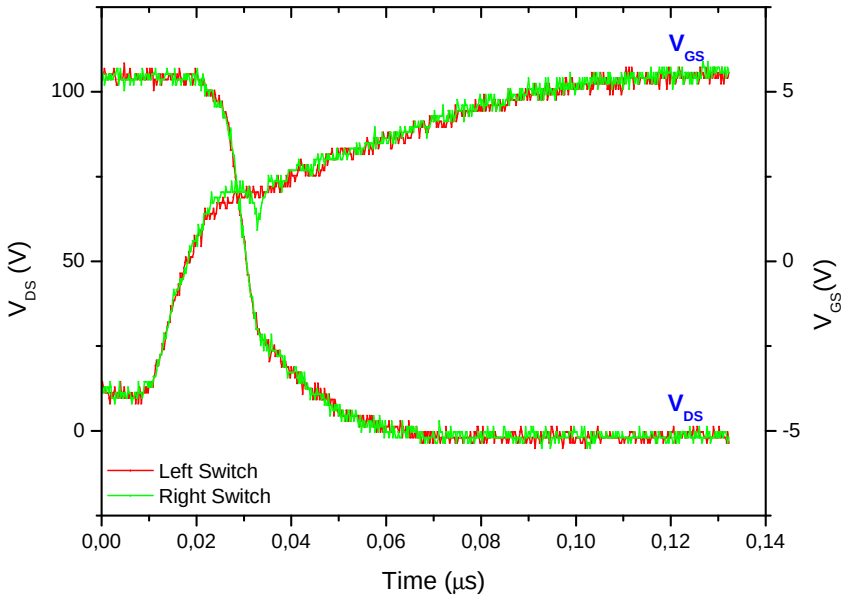
Figure 4.9: Gate resistor placement for parallel transistor operation

Table 4.2: Layout inductances for parallel connected transistors

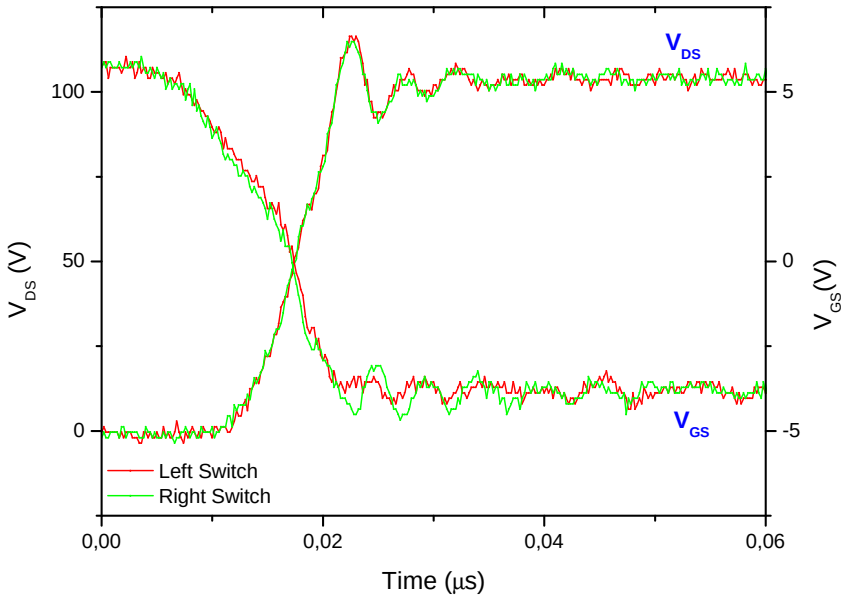
	Left Transistor	Right Transistor	Difference
Power Loop Ind.	0.87 nH		-
Positive Gate Loop Ind.	4.14 nH	4.23 nH	2.1%
Negative Gate Loop Ind.	3.88 nH	4.04 nH	4%
Mutual Ind.	0.114 nH	0.117 nH	2.5%

actual design and the results are given in Table 4.2. A very low power loop inductance as 0.87 nH is obtained. More important than the decreased power loop inductance, gate loop inductances and mutual inductances between the power loop and the gate loops differ less than 5% for parallel-connected transistors. Note that gate loop inductances are higher for the parallel connected case because, in this configuration, the minimization is sacrificed for obtaining equal inductances. However, the parasitic loop inductances which are given in Table 4.2 are not that harmful as shown in the experimental results.

In Fig. 4.10, turn-on and turn-off waveforms are given for parallel-connected transistors. The right and left switch turn-on and turn-off simultaneously, which is a clear indicator of even distributed layout parasitics. Lastly, double pulse test (DPT) results are presented in Fig. 4.26. Transistors are switched with 20 Ω and 2 Ω turn-on and turn-off gate resistances, respectively. Whenever the control switch is turned on, the gate-source voltage of the synchronous switch is charged via Miller capacitance as presented in Fig. 4.5. As shown in Fig. 4.26, the gate-source voltage is charged up to



(a) Turn-on



(b) Turn-off

Figure 4.10: Turn-on and turn-off waveforms of parallel connected switches

-2.2 V which stays lower than the threshold level, 1.7 V. This is a result of optimized and decoupled power loop and gate loop layouts.

4.2 Short Circuit Protection

GaN HEMTs are extremely susceptible to circuit noise due to their low threshold levels [51]. This sensitivity requires a very careful layout design in order to eliminate the risk of false turn-on, [9], which can trigger a short circuit (SC) fault. In order to maintain safe operation, a fast and reliable SC detection method is necessary. The protection technique should be capable of detecting the fault and ceasing it in less than 500 ns if the DC bus voltage is higher than 350V [28].

In this design, the protection method, sensing the voltage across by layout inductance, proposed in [35] for single GaN HEMT half-bridge configuration, is applied on a more developed half-bridge design where transistor paralleling is also applied for high-power applications. A hard switching fault (HSF) type SC fault can damage the multiple numbers of GaN HEMTs for a parallel-connected structure which increases the cost of failure. In order to implement this SC protection, the power loop inductance and the SC current sensing coupling inductance are characterized using a finite element analysis (FEA) tool. Also, a soft turn-off mechanism is employed to eliminate any risk of over-voltage breakdown when SC current is ceased. Experimental results show that this method does not deteriorate the layout inductance and it is capable of detecting HSF type SC fault in less than 40 ns. GaN HEMTs are completely turned off in less than 250 ns which ensures the safety of operation.

4.2.1 Theory of Operation

When a shoot-through type SC occurs, the bypass capacitors discharge through the transistors on the half-bridge. The stored energy on those capacitors leads SC current to reach harmful levels just in 100 ns to 200 ns. This energy transfer happens based on the components and circuit characteristics such as bus capacitance and impedance of the current path, i.e. the PCB layout. The inductance of this path is called the power loop inductance. Even though a minimized power loop inductance results in a sharp

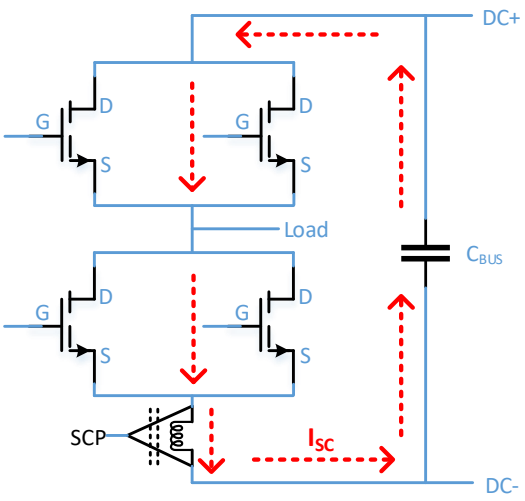


Figure 4.11: Circuit schematic of half-bridge

increase in SC current, it should be minimized for the normal switching operation.

4.2.2 Sensing SC Fault

As shown in Fig. 4.11, the power loop is a closed current path which can be considered as tip to tip connected small layout portions. Note that, whenever an SC happens, all current flows through those portions as well. Since the change in current induces a voltage on an inductance, a portion of the PCB layout can be used as a trigger for a short-circuit protection (SCP) mechanism as illustrated in Fig. 4.12 without increasing the power loop inductance.

However, the circuit dynamics of an SC fault is more complex due to mutual couplings and the second-order effects. Fig. 4.12 shows how a SC current induces the sensing voltage, V_{sense}. The power loop bus capacitor (C_{BUS}) and GaN HEMTs are segregated from DC supply with large connection inductances (L_{CON}) which do not allow a sharp rise on the current drawn from the voltage source. Therefore, SC current is mainly supplied by the energy stored on the power loop bus capacitor. SC fault occurs when a switch gets conductive while it is supposed to be OFF. An illustration of this situation is given in Fig. 4.12 where the low side switch is turned-on unintentionally. The rise of SC current depends on how fast the transistor gets fully

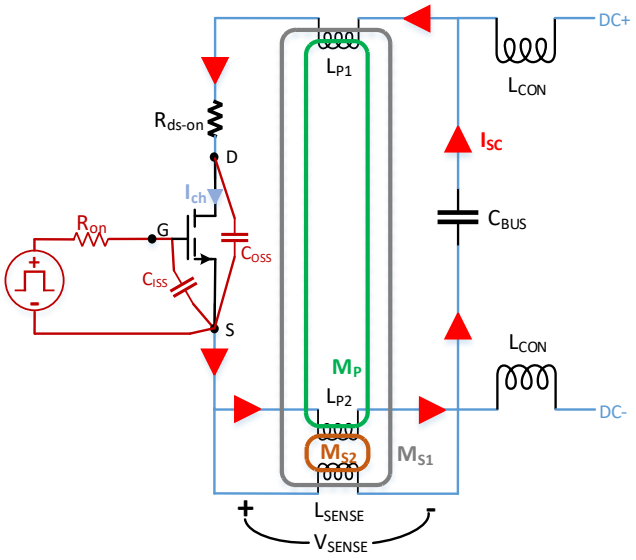


Figure 4.12: Dynamics of SC fault sense circuit

conductive, the path inductances, and series resistances. When the input capacitance (C_{iss}) of a transistor is charged, the trans-conductance (g_m) of the channel increases until it reaches the saturation. Simply ignoring the gate loop inductance, the charging speed of input capacitance depends on turn-on resistor (R_{on}) and input capacitance (C_{iss}) as given in (4.3). The gate voltage of the transistor is charged from OFF level (V_{low}) to the ON level (V_{high}). The OFF level is set below 0 V to eliminate a false turn-on risk [9]. With the increasing voltage of input capacitance, the transistor operating point moves from cut-off to saturation region. The relation between gate-source voltage, drain-source voltage and drain current (trans-conductance) is characterized by the manufacturer [52] as in (4.4).

$$V_{gs}(t) = (V_{high} - V_{low})(1 - e^{\frac{-t}{R_{on}C_{iss}}}) + V_{low} \tag{4.3}$$

$$I_{ds} = K_1(T)\ln(1 + e^{\frac{V_{gs}-V_{th}}{K_2}})\frac{V_{ds}}{1 + \max(K_3 + K_4(V_{gs} + K_5), K_6)V_{ds}} \tag{4.4}$$

When the gate-source voltage exceeds the threshold level of the transistor, the current starts to rise and then circuit dynamics gain importance. One of the key components of the current path is the power loop inductance (L_P), which is shown in two parts as L_{P1} and L_{P2} in Fig. 4.12. L_{P2} represents the portion of the power loop where the

SC fault sense loop is connected across and L_{P1} is the rest portion of the power loop. However, power loop inductance is not equal to the sum of these two inductances due to mutual coupling between them (M_P). The equivalent inductance of two series-connected inductors, L_{P1} and L_{P2}, can be expressed as in (4.5). The actual value of L_P can be found by finite-element-analysis (FEA) simulation.

$$L_P = L_{P1} + L_{P2} - 2M_P \tag{4.5}$$

In order to identify the parameters affecting SC current, the circuit KVL equation has to be solved. The voltage on the bottom side switch can be expressed as in (4.6). It can be considered that the SC current splits into two parts inside the transistor between the output capacitor C_{oss} and transistor channel I_{ch} as given in (4.7). The voltage on the drain-source terminal can also be expressed as in (4.8). The equation (4.6) can be expressed as in (4.9) by using (4.7) and (4.8). Since C_{oss} is a capacitance in the range of pFs, the terms with C_{oss} can be simply ignored, which means the current passing through output capacitance is much lower than the channel current. Therefore, (4.9) can be simplified as (4.10). The second-order differential equation of SC current can be formulated as in (4.11) by taking time derivative of (4.10). Even though nonlinear trans-conductance and its time derivative makes that differential equation hard to solve, it shows that SC current depends on the on-state resistance of high side switch (R_{ds-on}), the trans-conductance of low side switch (g_m), power loop inductance (L_p), bus capacitance (C_{bus}) and charging speed of gate-source voltage (V_{gs}). In other words, SC current depends on gate charging resistance (R_{on}) and input capacitance (C_{iss}) as derived in (4.12). Note that L_{sense} does not carry the SC current because it is relatively high in comparison to the power loop inductance.

$$V_{ds}(t) = V_{DC} - \frac{1}{C_{bus}} \int_{t_o}^{t} I_{sc}(t)dt - L_p \dot{I}_{sc}(t) - R_{ds-on} I_{sc} \tag{4.6}$$

$$I_{ch} = I_{sc} - C_{oss} \dot{V}_{ds}(t) \tag{4.7}$$

$$V_{ds}(t) = g_m I_{ch} \tag{4.8}$$

$$\frac{1}{C_{bus}}\int_{t_o}^{t} I_{sc}(t)dt + I_{sc}(g_m + g_m\frac{C_{oss}}{C_{bus}} + R_{ds-on}) + \\ \dot{I}_{sc}(t)(L_p + g_m C_{oss} R_{ds-on}) + \ddot{I}_{sc}(t) g_m C_{oss} L_p = V_{DC} \tag{4.9}$$

$$\frac{1}{C_{bus}}\int_{t_o}^{t} I_{sc}(t)dt + I_{sc}(g_m(V_{gs}) + R_{ds-on}) + \dot{I}_{sc}(t)L_p = V_{DC} \tag{4.10}$$

$$\ddot{I}_{sc}(t)L_p + \dot{I}_{sc}(t)(g_m(V_{gs}) + R_{ds-on}) + I_{sc}(t)(\dot{V}_{gs}(t)\dot{g}_m(V_{gs}) + \frac{1}{C_{bus}}) = 0 \tag{4.11}$$

$$\dot{V}_{gs}(t) = \frac{V_{high} - V_{low}}{R_{on}C_{iss}} e^{\frac{-t}{R_{on}C_{iss}}} \tag{4.12}$$

The SC current induces a voltage on the sense loop because it is coupled to the power loop as shown in Fig. 4.12. M_{S1-2} are the coupling inductances between L_{P1-2} and L_{sense}. Similar to equivalent power loop inductance the mutual inductance between L_P and L_{sense} can be expressed as M_{PS} which equals to the difference of two mutual couplings as given in (4.13). This mutual coupling can be characterized by FEA software. Rather than self inductances, mutual coupling induces the voltage on sense loop under an SC fault. Therefore, it is not necessary to have a large power loop inductance to obtain detectable levels of the induced voltage. Low power loop inductance can be utilized as long as the mutual coupling between the power loop and the sense loop is enough.

$$M_{PS} = M_{S2} - M_{S1} \tag{4.13}$$

4.2.3 Evaluating and Removing SC Fault

The induced voltage on the sense loop due to SC current can be processed to detect SC faults. For this purpose, firstly, the sensed voltage, V_{sense}, is filtered through a low-pass filter and it is compared with a reference level, V_{ref}, to detect SC fault as given in Fig. 4.13. Whenever an SC fault is detected, a high-frequency micro-controller

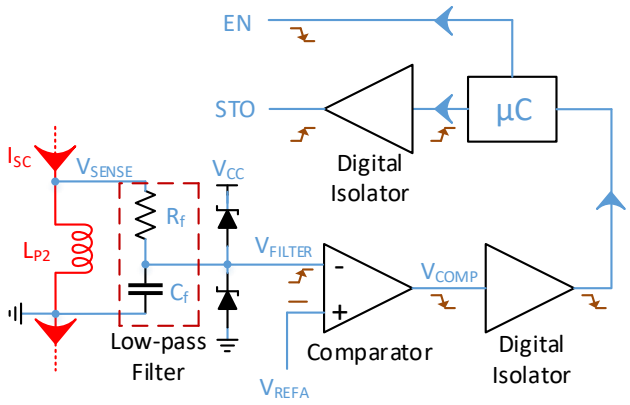


Figure 4.13: Short circuit protection mechanism

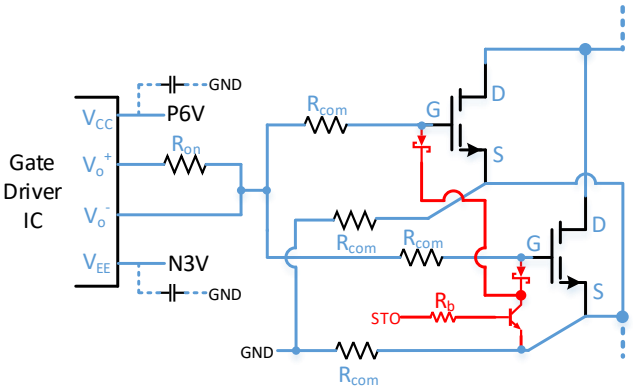


Figure 4.14: Gate driver circuit schematic of parallel connected transistors (red components exist only for low side transistors for soft turn-off (STO))

(μC) is triggered to protect the circuit. The μC activates the soft turn-off mechanism (STO) in order to diminish gate-source voltages of transistors. STO signal is applied to the base of a Bipolar Junction Transistor (BJT) which is connected between gate and source terminals of parallel-connected transistors as shown in Fig. 4.14. Base resistor, R_b, allows controlling discharge time of stored gate charge. Therefore, the turn-off speed of GaN HEMTs can be controlled. After the soft turn-off process is completed, the gate driver integrated circuit (IC) is disabled which results in complete turn-off.

A direct hard turn-off poses a great risk of over-voltage breakdown. Although hard turn-off (HTO) stops SC current immediately, it causes a voltage induction on power loop inductance as happened in the regular switching operation. Since the SC current

reaches extremely high levels, applying HTO causes high voltage induction which can go beyond the voltage rating of transistor easily. Therefore, a soft turn-off mechanism must be used and a BJT is used for this purpose in this design. As given in Fig. 4.14, a Schottky diode is connected in series with BJT since the negative drive level of gate-source terminals could bias the NPN type BJT in the reverse direction.

As shown in Fig. 4.14, a single BJT is used to ensure that parallel-connected transistors will be turned off simultaneously. Otherwise, SC current might have to be carried by only one of them. Note that, SCP mechanism components and soft turn-off BJT are placed on the low side of half-bridge because switching node has a varying voltage level. The rapid voltage transitions on the switching node could risk the common-mode transition immunity (CMTI) ratings of isolated components and therefore, the digital signals might change their states unpredictably.

4.2.4 SC Protection Design Integrated to a Half-Bridge

A prototype of the parallel switch half-bridge board with short circuit protection is presented in Fig. 4.2. In this design, GS66508T GaN HEMTs (650 V, 30 A) are used as the device under test (DUT). The PCB is designed in a similar manner to the manufacturer's evaluation board [53]. Even though this half-bridge is designed for a 4 kW bidirectional DC/DC converter operation, it can be used for different purposes. The multiple numbers of this half-bridge can be used to have different types of DC/DC converter or an inverter. The dimensions of the half-bridge board are 90 mm (L), 40 mm (H), and 30 mm (W) with heat-sink and fan.

4.2.5 SC Protection Integrated Layout Design

A proper power loop layout design is critical for safe operation, especially for GaN HEMTs considering their rapid switching transition. Additionally, it is important to estimate the induced voltage on the loop portions under SC fault for accurate detection. For this purpose, the Finite Element Analysis (FEA) tool is required to solve and analyze the complex geometry of the PCB layout. In this design, the ANSYS Maxwell 3D tool is used for identifying PCB characteristics.

First of all, a basic representation of the PCB layout is shown in Fig. 4.15. The current return path is placed underneath of top copper layer so that the power loop inductance could be minimized. Also, the induced voltage on a portion of the return path is sensed, which is defined as the sense loop. Moreover, a simplified geometry of these two loops can be modeled as given in Fig. 4.16. The current, which flows through the power loop, induces a voltage on the sense loop with a coupling factor of M_{PS}, as presented in (4.14). In order to identify the coupling factor, the change rate of power loop current is used as a control variable. According to Ampére's law (4.16) in quasi-static form, the current density, (4.15), creates a magnetic field ($\vec{B}$) which passes through the sense loop. The total flux linkage can be calculated based on Gauss's Law of Magnetism as in (4.17). The time derivative of total flux linkage within the loop area induces a voltage which is a result of Lenz's Law of Induction, (4.18).

$$\varepsilon = M_{PS}\frac{\partial i_{SC}}{\partial t} \tag{4.14}$$

$$i_{SC}(t) = \int_S \vec{J}.d\vec{S} \tag{4.15}$$

$$\mu_0 \oint_l \vec{B}.d\vec{l} = \int_S \vec{J}.d\vec{S} \tag{4.16}$$

$$\Psi = \int \vec{B}.d\vec{A} \tag{4.17}$$

$$\varepsilon = -\frac{\partial \Psi}{\partial t} \tag{4.18}$$

Similar to the simplified model, the sensed voltage on the PCB can be calculated by estimating the total flux linkage in the sense loop as shown in Fig. 4.17. For this purpose, the magnetic field density vectors ($\vec{B}$) passing through the sense loop and created by power loop current for 100 A are solved with an FEA software and shown in Fig. 4.18. According to FEA results, the power loop current induces voltage with a mutual coupling factor, M_{PS}, of 0.18 nH. Also, the self-inductance of the power loop layout is 0.85 nH. The FEA results show that the power loop inductance is not necessarily increased to obtain an evaluable sense voltage level.

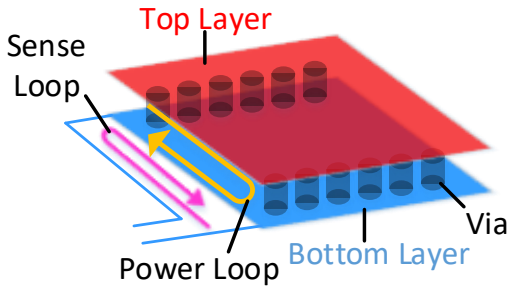


Figure 4.15: A symbolic view of PCB layout for power loop and sense loop

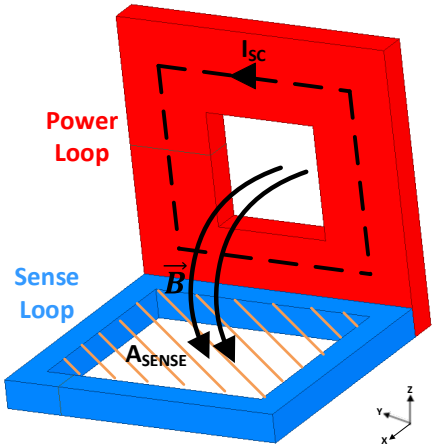


Figure 4.16: A simplified model of PCB layout for power loop and sense loop

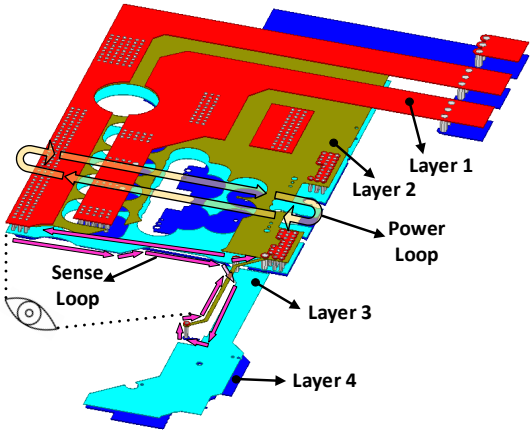


Figure 4.17: Layout view for power loop and sense loop where layer orders are given from top layer (Layer 1) to bottom layer (Layer 4)

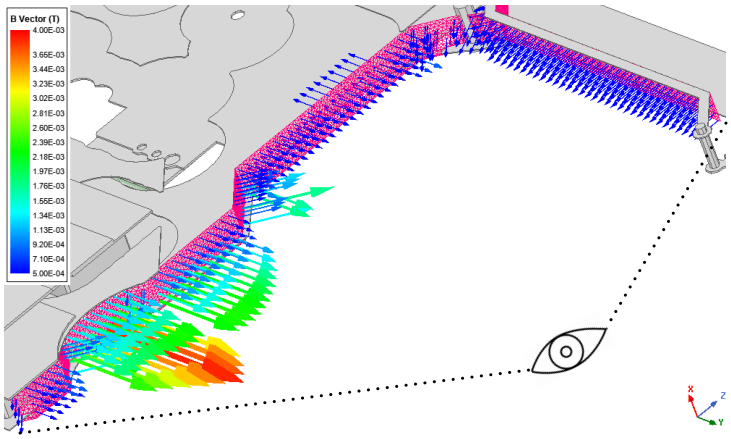


Figure 4.18: Magnetic field density vectors passing through sense loop created by 100 A power loop current

4.2.6 Filter Design

The induced voltage waveform has to be filtered to eliminate any mis-trig signal caused by regular switching. The main difference of induced voltages for regular switching and SC fault is the oscillation frequency. According to simulation results, the transistor current continues to increase for a while under an SC fault whereas for normal operation, the current reaches the peak and then decreases as shown in Fig. 4.19. Moreover, the shaded areas under induced voltages show the integration fields. On the one hand, the integration adds up steadily for the SC fault case. On the other hand, the induced voltage oscillates between positive and negative sides for normal switching, so it does not add up invariably. Therefore, a low pass filter that accumulates the induced voltage would satisfy the required filtering characteristics. For this purpose, an R-C filter is used as presented in Fig. 4.13. The KVL equation for an R-C filter (4.19) can be transformed and the voltage on the capacitor, V_{filter}, can be expressed as in (4.20) where the integration of induced voltage is obtained.

$$v_{sense}(t) = v_{filter}(t) + C_f \frac{\partial v_{filter}(t)}{\partial t} R_f \tag{4.19}$$

$$v_{filter}(t) = \frac{1}{R_f C_f} \int_0^t (v_{sense}(t) - v_{filter}(t)) dt \tag{4.20}$$

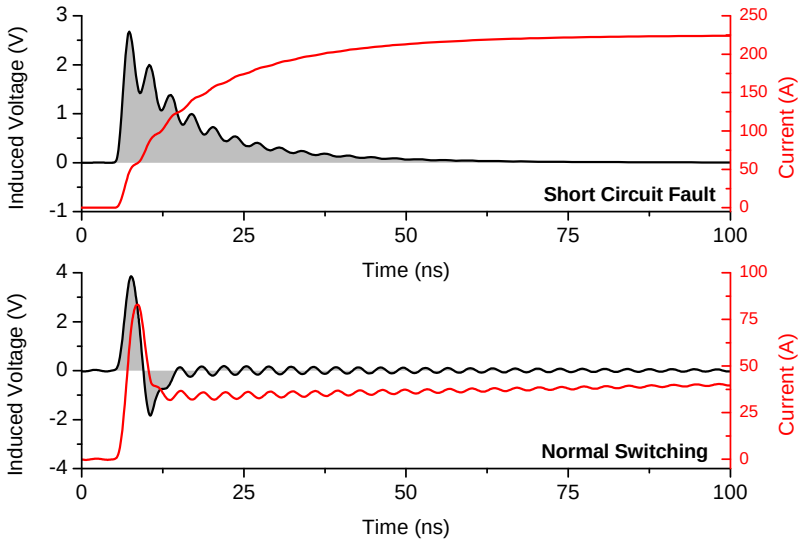


Figure 4.19: Comparison of power loop currents (I_{L_P}) and induced voltages (V_{sense}) for short circuit fault and normal switching

The FFT results of induced voltage (V_{sense}) for short-circuit fault and normal switching are given in Fig. 4.20 based on simulation results. The normal switching dominates on the FFT plot as frequency increases due to high-frequency oscillations. However, for the low-frequency range ($<$ 25 MHz), the amplitude is much higher for SC fault, so it is the frequency range to be passed by the filter. Three different filter options are compared in Fig. 4.21. It is possible to change the location of the cutoff frequency by changing either R_f or C_f. As given in Fig. 4.21, all R-C filter options are strongly attenuate for frequencies higher than 25 MHz. 10Ω - 1nF combination could be the best option for having a comparable voltage level but in comparison to simulation, the actual waveform should have more oscillations in real experiments due to the parasitic effect which cannot be perfectly modeled in a simulation environment. Therefore, 10Ω - 1nF might not be enough to attenuate all those oscillations. Also, 30Ω - 1nF would be a very tight filter to have a voltage at a comparable level, so noise in the system can easily cause a mis-trig. Therefore, it is a good choice to have a filter around 20Ω - 1nF, and the following experiments are conducted with a filter with 18Ω - 1nF component ratings.

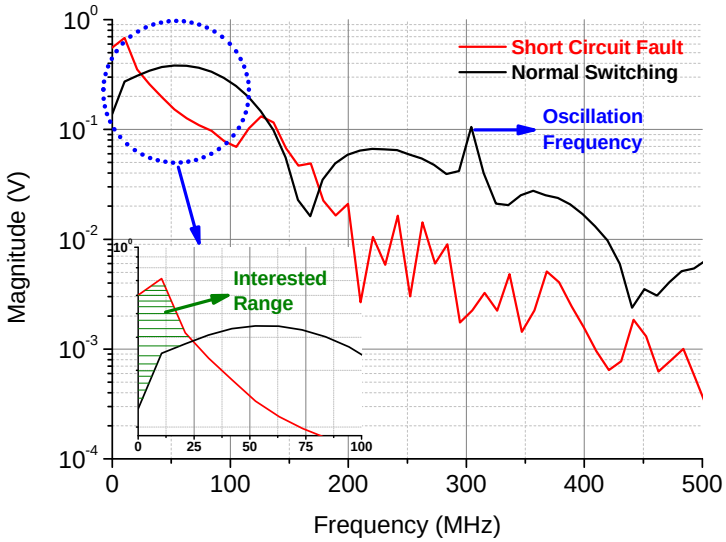


Figure 4.20: FFT plots of induced voltage (V_{sense}) for short circuit fault and normal switching operation (A zoomed version of the circled region is presented on the same figure at the bottom)

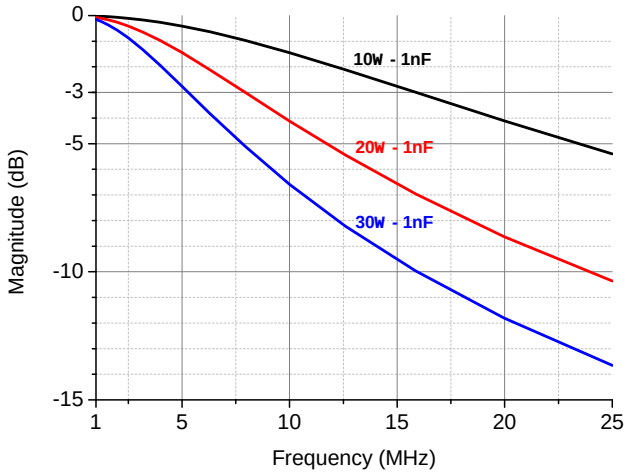


Figure 4.21: Magnitude plot of three different low-pass R-C filters

4.2.7 Component Selection

As shown in Fig 4.13, a comparator is required to have a digital trig. For this purpose, a fast comparator TLV3501 with 4.5 ns delay is used. Also, a digital isolator

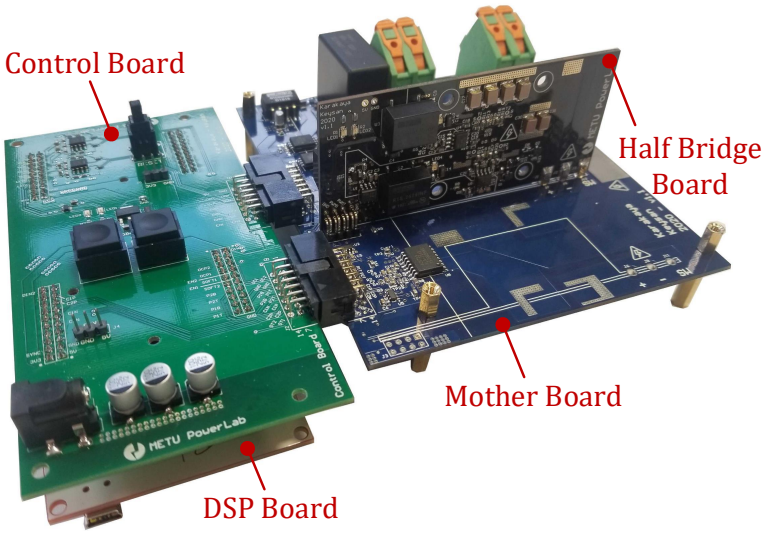


Figure 4.22: Experimental setup for SC protection test including a DSP board, a control board, a mother board and the half-bridge board

is required to transfer the signal from the power side to the signal side or vice versa. The digital isolator should also be able to stand with high common-mode interference. Therefore, ISO7721 with 11 ns propagation delay and 85 $kV/\mu s$ common-mode transient immunity is selected.

Moreover, to safely turn-off GaN HEMTs, a Bipolar Junction Transistor (BJT) is implemented to clamp gate-source voltage. ZXTN19020DFF with a static forward current transfer ratio of 450 is utilized and a 1 kΩ base resistor is used to adjust clamping duration.

4.2.8 Experimental Results

The half-bridge board is tested in a configuration as given in Fig. 4.22. A digital signal processor, TMS320F28379D, with 200 MHz clock speed is used for generating PWM signals and for applying short-circuit protection. Experiments are organized to show the capability of the SC protection mechanism and the regular switching performance of the half-bridge board.

As shown in Fig. 4.23, SC fault is detected just in 40 ns and the transistors are com-

pletely turned off in less than 250 ns with soft turn-off in an SC fault case described in Fig. 4.12. The time intervals are measured experimentally with a LeCroy Waverunner 44-Xi (400 MHz, 5 GSa/s) oscilloscope. The induced voltage (V_{sense}) under SC fault increased up to 1.2 V. Therefore, SC current increased with a slope of 6.7 A/ns as maximum. The measurement of SC current requires a high-bandwidth current measurement technique. In [54], different options for measurement of switching current of GaN transistors are compared. The most suitable technique is to utilize a shunt resistor with ultra-high bandwidth (2 GHz). However, even this method adds several nH parasitic inductances into the power loop inductance [54]. Considering the power loop inductance of proposed design, 0.85 nH, a high-bandwidth shunt resistor could increase power loop inductance more than 100%. Therefore, the SC current is not shown experimentally in Fig. 4.23 because it cannot be measured without changing the layout inductance. A worse power loop design would harm or completely change or invalidate the performance of the SC protection mechanism.

In Fig. 4.23, time steps of an SC fault are shown in detail. When an SC fault starts with an unexpected turn-on of a transistor, drain-to-source voltage (V_{ds}) waveform shows a voltage drop because of the drawn high current from the power loop bus capacitors. The high rise of the SC current induces a voltage (V_{sense}). Filtered form of the induced voltage (V_{filter}) exceeds the reference level (V_{ref}) and as a result, comparator output (V_{comp}) changes its state to low, which is the moment of SC fault detection ($t_1 + t_2$). Then, this signal is transferred to DSP with the digital isolator. DSP first sets soft-turn off command, so gate-to-source voltage (V_{gs}) starts discharging. After 250 ns from SC fault start, (V_{gs}) is totally clamped to a level below threshold voltage which means SC fault is removed. Then, DSP waits for a programmable awaiting duration and disables gate drivers, so gate driving level goes to low state. The delay intervals in SC timing waveform are affected by several factors positively or negatively as given in Table 4.3. In order to minimize short-circuit, protection duration, a fast comparator IC and a fast digital isolator IC are required. Even though the total SC protection duration is dominated by the soft turn-off period, the SC current decreases gradually with time and soft turn-off is a must for safe operation. A comparison result is shown in Fig. 4.24. For a hard turn-off situation, the voltage on GaN HEMTs increases up to 105 V under 50 V_{DC} input which clearly indicates the risk for a higher

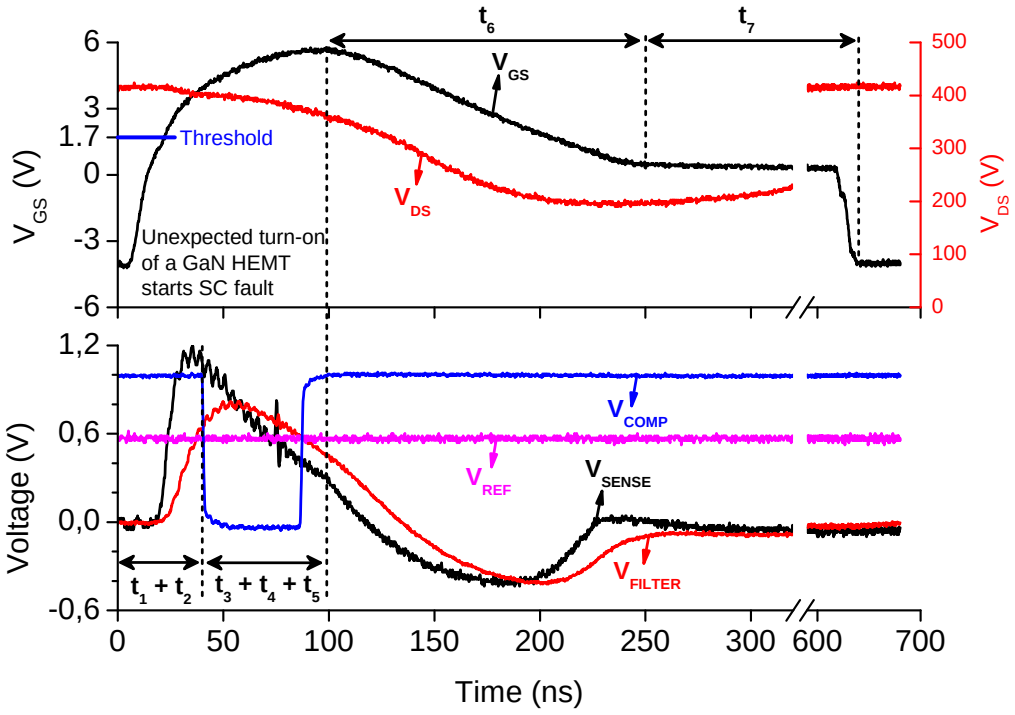


Figure 4.23: Unexpected turn-on of a GaN HEMT starts SC fault: Timing waveform of SC protection mechanism under 400 V bus voltage where V_{gs} and V_{ds} are the gate-source and drain-source voltage of bottom switch, V_{sense} is the induced voltage on PCB layout, V_{filter} is the low-pass filtered form of V_{sense}, V_{ref} is the threshold level of SC signal and V_{comp} is the scaled output of comparator IC.

level of input voltages. On the contrary, when a soft turn-off is applied, the voltage on GaN HEMTs does not increase more than the bus voltage and it ensures a transition in safe-operating-area limits.

Furthermore, the waveforms of induced voltage (V_{sense}) and its filtered form (V_{filter}) during an SC fault are measured under different bus voltage levels and given in Fig. 4.25. All bus voltage levels result in the same amount of voltage induction because the transistor current gets in saturation for all voltage levels which means the same trans-conductance for all voltage levels. These results also highlight the SC fault detection range. The SC fault can be detected as long as the bus voltage is high enough to bring transistors in saturation.

Besides SC fault results, double pulse test (DPT) results are presented in Fig. 4.26,

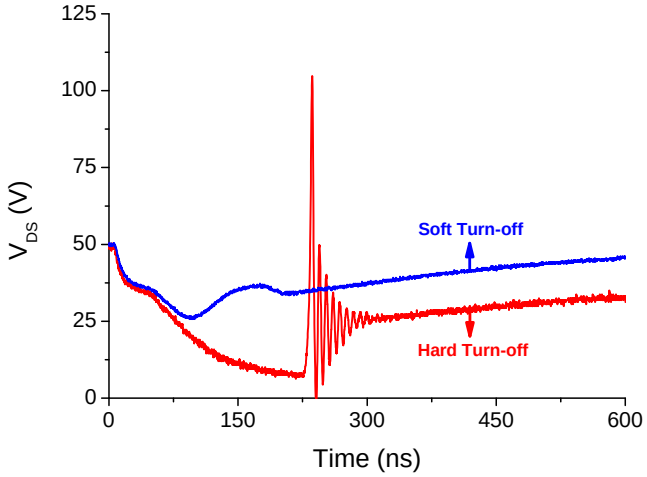


Figure 4.24: Bottom side transistor drain-source voltages for hard and soft turn-off situations under 50 V DC bus voltage SC test

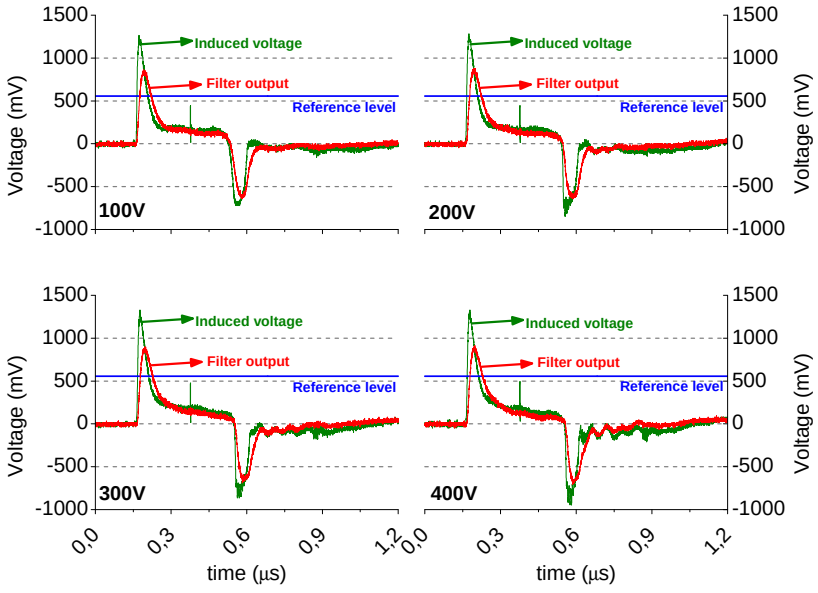


Figure 4.25: Induced voltage (V_{sense}) and filtered waveforms (V_{filter}) for SC fault under varying DC bias levels

Table 4.3: Delays and Related Factors During SC Fault

Time Interval	(ns)	Prolonging Factors	Expediting Factors
t_1	35	Loop Inductance Filter Components	Bus Capacitance
t_2	5	Comparator Delay	-
Detection	40	-	-
t_3	11	Isolator Delay	-
t_4	37	Interrupt Latency	DSP Clock Speed
t_5	11	Isolator Delay	-
Turn-off Start	99	-	-
t_6	151	Base Resistor	BJT Gain
Total	250	-	-
t_7	390	Programmable awaiting duration	

for 400 V and 40 A to show normal switching performance and clarify the differences between SC fault and normal switching. Transistors are switched with 20 Ω and 2 Ω turn-on and turn-off gate resistances causing 22.8 $kV/\mu s$ and 40.7 $kV/\mu s$ average transition speed, respectively. Whenever the control switch is turned on, the gate-source voltage of the synchronous switch is charged via Miller capacitance. As shown in Fig. 4.26, the gate-source voltage is charged up to -1.8 V which stays lower than the threshold level, 1.7 V. This is a result of optimized and decoupled power loop and gate loop layouts. It also shows that the protection method does not deteriorate the layout design. For the same switching moments, the induced voltage (V_{sense}) and filtered waveform (V_{filter}) are also shown in Fig. 4.26. As expected, V_{sense} is much noisier in comparison to the simulation result. Nevertheless, the filter is able to attenuate those high-frequency oscillations and V_{filter} never exceeds the reference level and does not cause a false trigger. In addition, the V_{filter} waveforms are presented in Fig. 4.27 for different DC bias levels and loading conditions. In all situations, the V_{filter} does not

reach and exceed the reference level.

In order to see the noise immunity better, the FFT results are given in Fig. 4.28 where FFT results of induced voltage (V_{sense}) and its filtered form (V_{filter}) are compared for normal switching and under SC fault. As explained in Section 4.2.6, normal switching carries more high-frequency components but SC fault dominates for frequencies lower than 25 MHz in experimental results as well. These results also validate filter design.

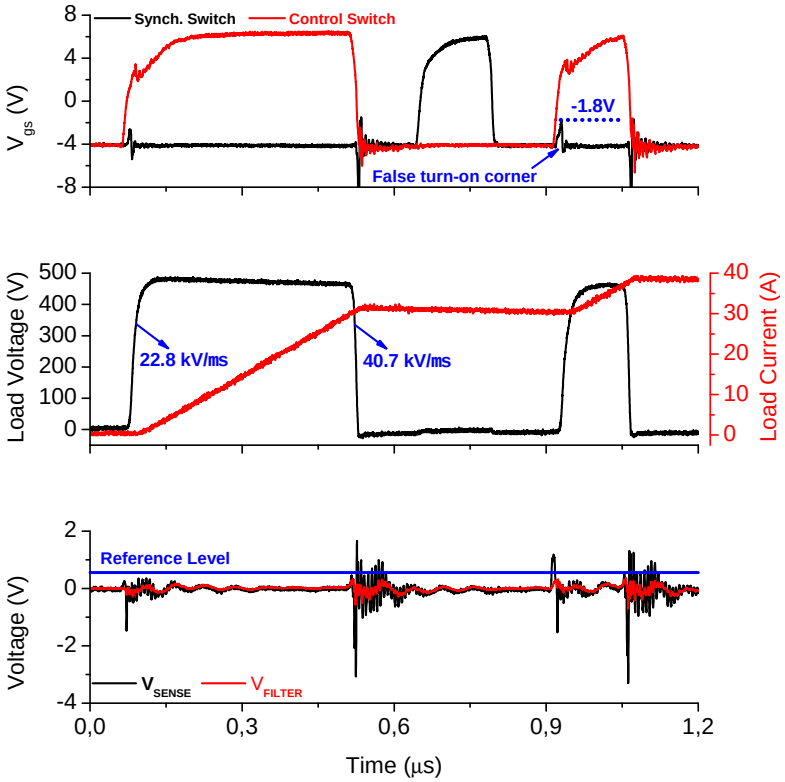


Figure 4.26: Double Pulse Test (DPT) waveforms: applied pulses to the gate-source terminals of control & synchronous switches, the load current & voltage waveforms and induced voltage (V_{sense}) and its filtered form (V_{filter})

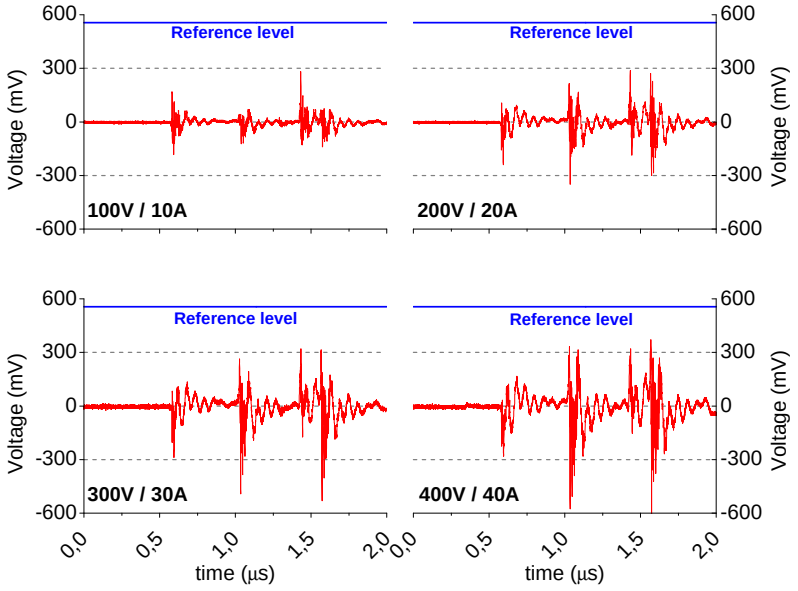


Figure 4.27: Filtered waveforms of induced voltage (V_{filter}) for DPT under varying DC bias levels and loading conditions

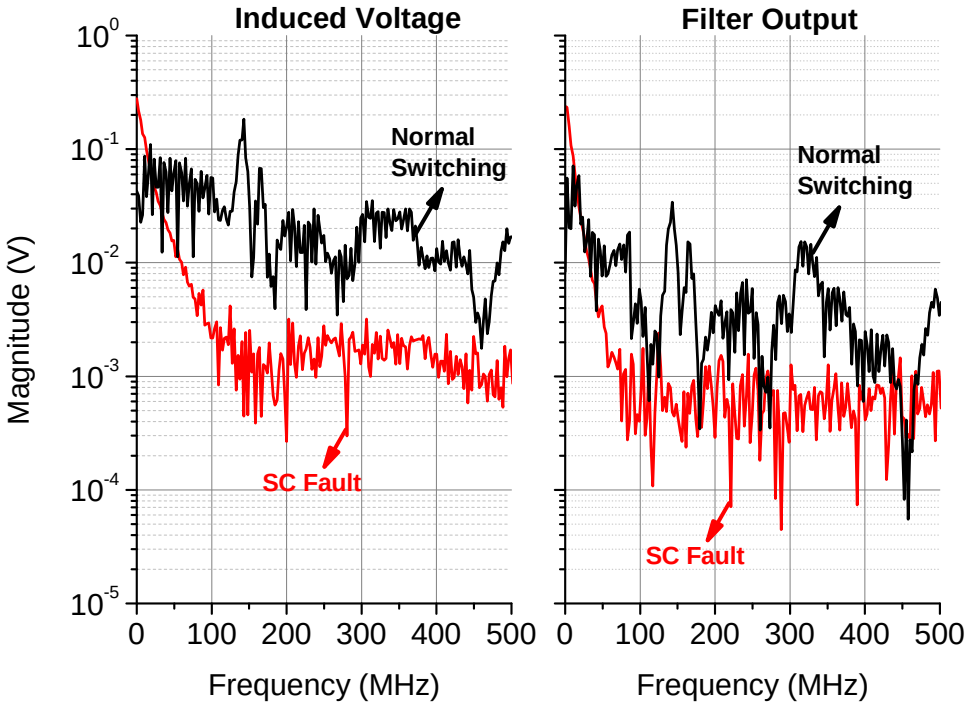


Figure 4.28: Comparison of FFT plots of induced voltage (V_{sense}) and its filtered form (V_{filter}) under SC fault and for normal switching conditions

4.2.9 Discussions

SC protection methods in literature and their performance are compared in Table 4.4. Those different sense techniques are shown in Fig. 4.29 as if they are applied on a parallel connection configuration. The small layout parasitic inductances are also placed on the figure. The SC fault is sensed with different methods such as drain-to-source voltage (V_{DS}) sense, bus voltage (V_{BUS}) sense, induced voltage sense across the common source inductance (CSI) or layout inductance. The STO activation, i.e. gate clamping, the delay is taken as a common measure of different studies. STO activation period is an important measure since it determines the duration of uncontrolled SC current rise. Even though the device type differs, all listed solutions in Table 4.4 are applicable to other types of devices except [30] as sensing the induced voltage across CSI requires a Kelvin source pin.

All of the reported studies are able to get SC current under control in less than 500 ns which is the critical limit for GaN HEMTs with 350 V or more DC bus voltage [28]. First six solutions in Table 4.4 are able to activate STO in less than 100 ns with 30 ns deviation as maximum. The proposed SC protection mechanism in this paper is designed and verified for parallel-connected GaN HEMTs and it starts STO in 99 ns and fault is removed completely in 250 ns in total.

The sensing methods other than the method proposed in this paper (3 in Fig. 4.29) might not be easily adapted to parallel configuration for several reasons. Firstly, the layout design considerations of parallel-connected transistors are different from single bridge design. Even though both designs aim to minimize gate loop and power loop inductances, it is required to distribute the layout inductances equally among parallel-connected transistors [23]. This requirement is critical to turn-on and turn-off the parallel-connected transistors at the same time. Therefore, the protection methods, which can follow only either one device or one bridge like options 1, 2, and 5 in Fig. 4.29, are inconvenient as they can cause asymmetry between parallel-connected transistors, which can make the switching speeds of parallel transistors dissimilar. These solutions can be adapted to the parallel configuration by increasing the number of sense points; however, this will increase the application cost and make the implementation difficult.

Table 4.4: SC fault response time of different protection methods applied on different device types and connections

Study	STO activ.	Sense	Device	Conn.
Hou et al. [33]	70 ns	V_{DS} (1)	GaN HEMT	Single
Sun et al. [30]	80 ns	CSI (2)	SiC	Single
Alemdar et al. [35]	80 ns	Layout (3)	GaN HEMT	Single
Hou et al. [6]	85 ns	V_{DS} (1)	GaN HEMT	Single
Awwad et al. [34]	90 ns	Layout (3)	SiC	Single
This work	99 ns	Layout (3)	GaN HEMT	Parallel
Lyu et al. [28]	200 ns*	V_{BUS}** (4)	GaN HEMT	Single
Wang et al. [32]	224 ns	V_{BUS}*** (5)	GaN GIT	Single

(*) STO activation period is measured by author using the waveforms presented in the paper

(**) Bus voltage is measured from positive terminal to negative terminal of power loop bus capacitor

(***) Bus voltage is measured from the drain of the high side switch to the source of the low side switch on a half-bridge

Secondly, the space limitations on the PCB lead designers to utilize different solutions even for single bridge configuration. An example is utilizing dual-gate pads separately for gate driving and soft turn-off as discussed in Chapter 1. Thus, the parallel connection of transistors complicates space limitations especially considering the strict layout design rules of parallel configuration.

Thirdly, it is not possible to obtain gate loop inductances as low as in single half-bridge design for parallel configuration. It is possible to place the gate driver IC just next to the transistor in a single configuration. However, due to symmetry considerations the gate driver IC cannot be placed next to a transistor. As a result, high gate loop inductance leads to higher oscillations on gate-source voltage, so on trans-

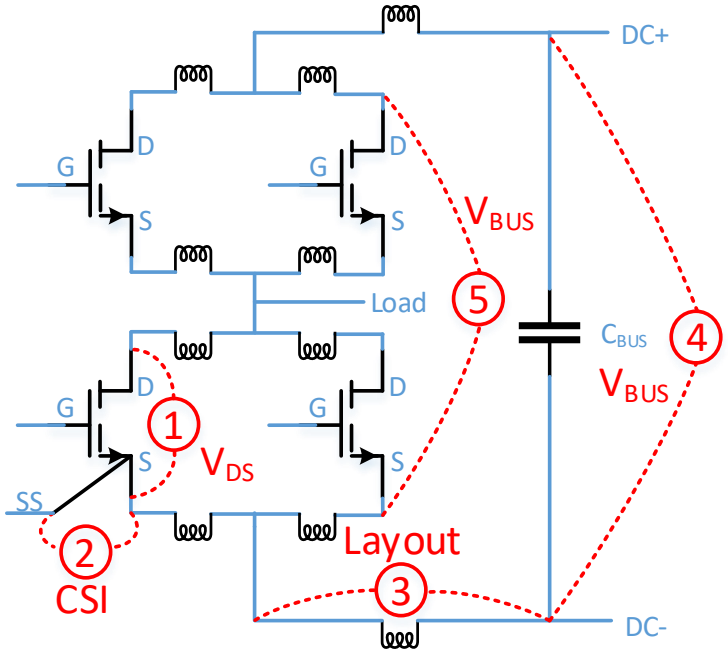


Figure 4.29: Different sense techniques to detect SC fault

conductance and transistor current as well. These oscillations require a tighter filter and long settling time.

Considering all these constraints, only bus voltage measurement technique across the bus capacitors other than the layout method can be adapted to the parallel configuration but it might not be easy to adjust reference levels for a different level of input voltages and according to Table 4.4, sensing bus voltage is the slowest technique. As a result, the layout based detection techniques are the most suitable methods to sense SC fault for parallel configurations.

4.3 Thermal Design

A proper power electronics design must include a thermal design for long period operations. The small size of the device package of GaN HEMTs makes it vulnerable to thermal loading. As the size gets smaller, it is hard to remove the heat. Therefore, thermal components should be selected with the device accordingly. Thermal com-

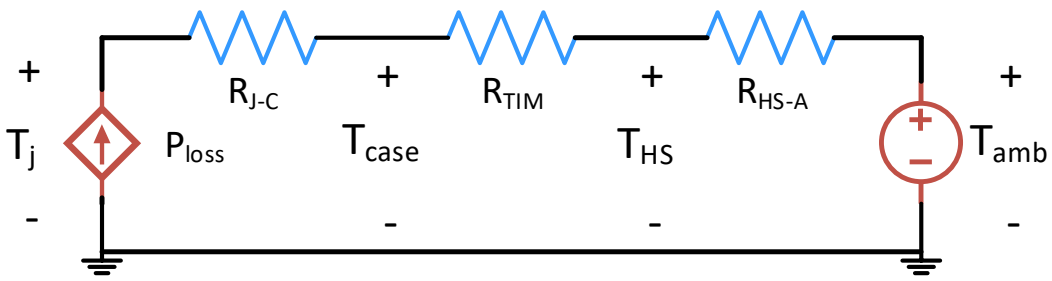


Figure 4.30: Single device thermal network

ponents include heat-sink, fan, thermal interface material which fills the gap between heat-sink and device. The Cauer thermal network is illustrated in Fig. 4.30 for a single device where R_{J-C} stands for the junction to case thermal resistance, R_{TIM} is the thermal resistance of thermal interface material and R_{HS-A} stands for heat-sink to ambient thermal resistance.

As mentioned in Section 4.1.3, use of parallel-connected two GaN HEMTs is advantageous than using a single device with a double current rating because of the wider contact area with the heat-sink. In the case of a single device, the heat is concentrated on a specific region of heat-sink but for parallel devices, the heat sources are separated.

The junction-to-case thermal resistance of the device is given as 0.5 °C/W in [4]. The total power loss of the transistors is calculated as 18 W using simulation results. The ambient temperature is assumed as 40 °C with some margin and the aimed junction temperature is 140 °C. Based on these starting points, the required total thermal resistance is found in (4.21) as 5.5 °C/W. Therefore, the total thermal resistance of R_{TIM} and R_{HS-A} should not exceed 5.5 °C/W to operate at 140 °C of junction temperature.

$$R_{total} = \frac{T_j - T_{amb}}{P_{loss}} \tag{4.21}$$

A thermal interface material (TIM), A10092-01 [55], with 0.25 $in^2°C/W$ thermal resistance per inch square (α_{TIM}) is selected for this operation. The equivalent contact area should be taken into account to find the actual thermal resistance of TIM. In this

case, it is the total cooling surface area of the transistors. The edges for this area is given as 0.257 inches and 0.122 inches in [4], so the cooling area is 0.125 in^2 in total. However, since the thermal conductivity of TIM is much greater in X and Y directions than Z direction, the effective contact area is larger and each edge is multiplied with 1.5 in calculations. As a result, TIM has a thermal resistance of 3.5 °C/W based on (4.22). Thus, a heat-sink with 2 °C/W is required. Considering the size of the PCB (90 mm (L), 40 mm (H)), it is not possible to have a heat-sink with the desired resistance for natural cooling. Therefore, a heat-sink and a suitable fan should be selected.

$$R_{TIM} = \alpha_{TIM} \frac{1}{A_{total} * 1.5^2} \tag{4.22}$$

A low-profile forged heat-sink, APF40-40-10CB [56], is selected with 2.5 °C/W thermal resistance at 200 LFM airflow where it causes 0.043 inch-water pressure drop. Therefore a fan should be picked which creates 200 LFM airflow under 0.043 inch-water pressure drop. OD3510-05MB [57] fan is selected and it is able to create 4.9 CFM or 285 LFM airflow under 0.04 inch-water pressure drop. Therefore, since the airflow is increased 42%, the thermal resistance of heat-sink will be lower. The heat-sink APF40-40-13CB [56] with 2.0 °C/W at 200 LFM can be a second option for certain limitations.

The heat-sink and fan are connected to PCB by screws as presented in Fig. 4.31. For this purpose, heat-sink is drilled in each corner aligned with the fan and they are tightly mounted on the PCB to have good contact between transistors and heat-sink. A loose contact might result in increased contact resistance and might cause a thermal run-away up.

In order to verify the thermal design, a controlled loss is applied to transistors and temperature variation on the heat-sink is followed by a thermal camera, FLIR E5 [58]. During these tests, all four transistors on the half-bridge are turned-on and continuous DC current flows through the transistors. The voltage on the transistors is measured to estimate power loss accurately. The voltage and power losses are shown in Fig. 4.32. During the tests, the current is increased up to 16 A and 16.6 W power loss is applied as the maximum which is equal to the estimated maximum loss in the actual

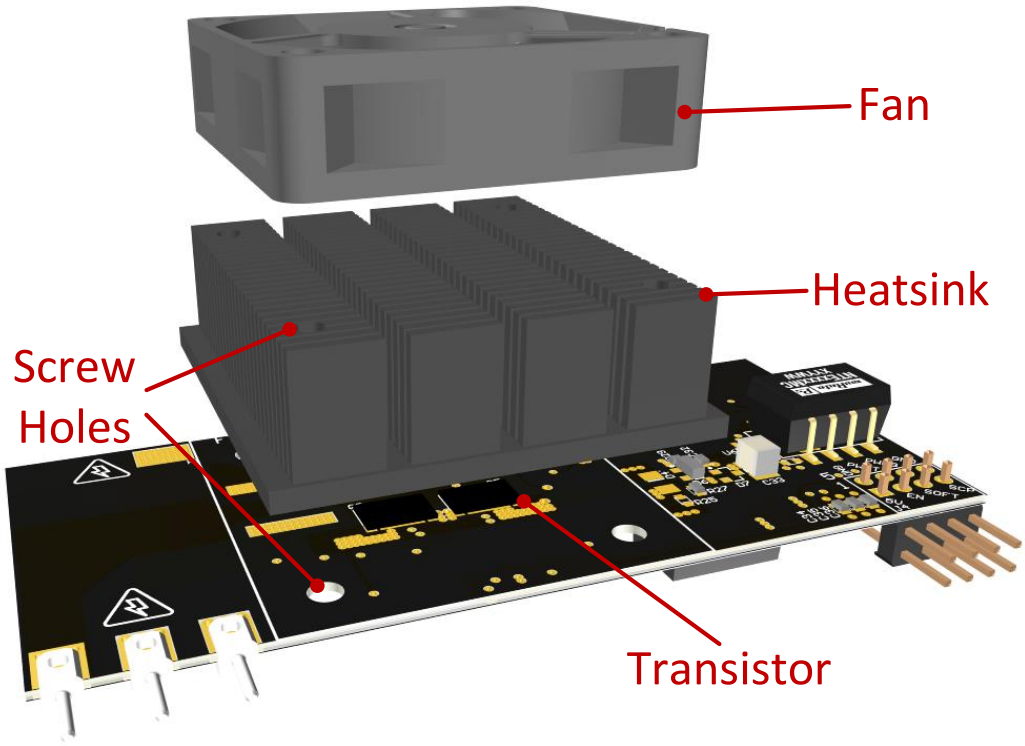


Figure 4.31: Connection of heat-sink and fan on PCB

circuit.

In order to match the power loss with the junction temperature, the temperature on the heat-sink is measured to calculate actual thermal resistance of it. Knowing the thermal resistances of all components (heat-sink, TIM, and junction-to-case), it is possible to estimate junction temperature under applied power losses. The estimated junction temperature is shown in Fig. 4.33 and it reaches to 133 $^{\circ}C$ maximum. Note that during the tests, the mounted heat-sink is APF40-40-06CB [56], which has 28% higher thermal resistance than the one that will be used. Additionally, the connected fan, OD3510-05LLB [57], is less powerful than the one that will be used. In short, thermal performance is verified with even less effectual heat-sink and fan. With those thermal results, the size of the half-bridge PCB is finalized as 90 mm length, 40 mm height, and 30 mm width.

As a conclusion, a prototype half-bridge design with GaN HEMTs is discussed in this chapter. The design of a half-bridge includes layout design, short-circuit protection integration, and thermal design. In the first place, the layout optimization for the

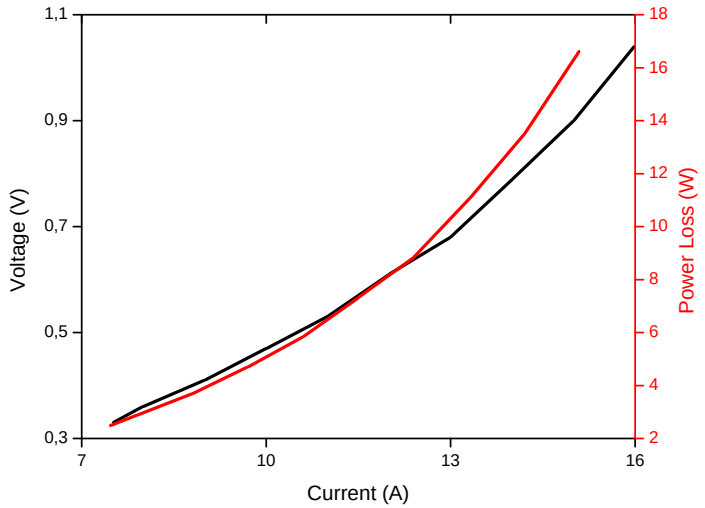


Figure 4.32: Applied losses in thermal tests

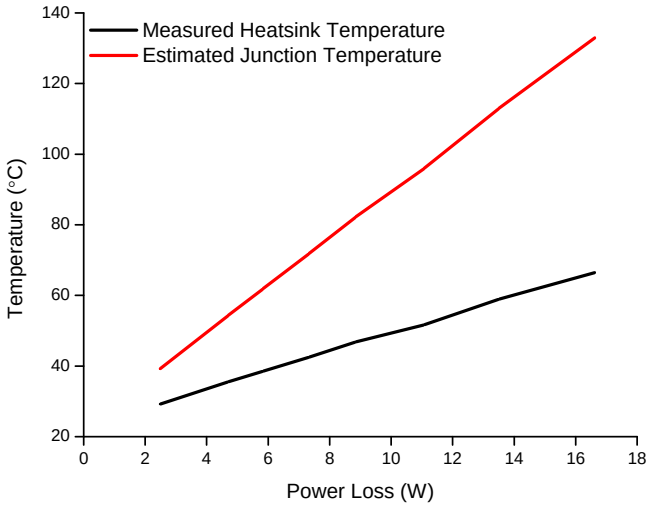


Figure 4.33: Measured heat-sink and estimated junction temperatures

power loop and the gate loop is discussed. Different design options are compared by FEA software. Then, the layout considerations for parallel-connected devices are described. A minimization of layout inductances is not enough for parallel devices, even distribution of parasitic inductances is also required. Experimental results show that a minimized and symmetric layout design is obtained on the proposed half-bridge.

Afterward, the implementation of short-circuit protection is given. The short-circuit protection has to be fast enough to inhibit a fault before device breakdown. The proposed method utilizes sensing the induced voltage on the layout. This method is able to detect SC fault in 40 ns and current is taken under control in less than 100 ns. Moreover, a unique piece of the SC method is that it is the first time an SC protection method is applied to parallel-connected GaN HEMTs. The proposed solutions in the literature are compared for parallel switch operation and the advantages of the layout method are presented.

Lastly, the thermal design of the half-bridge board is given with all details and experimental results. The selection of thermal interface material, heat sink, and the fan is discussed. The experimental results highlight that the half-bridge board is able to stand with at least 16 W of losses on GaN HEMTs.

CHAPTER 5

BI-DIRECTIONAL DC/DC CONVERTER DESIGN

The bi-directional DC/DC converters are used to construct an interface to energy storage systems. Especially, the increase in the usage of renewable energy sources requires energy storage systems like batteries where bi-directional power flow is required [40]. The buck/boost type bi-directional DC/DC converters are also used for onboard chargers and between the battery and the inverter bus of electric vehicles [39, 59], electric scooters or electric wheelchairs, and telecom energy systems [60]. In this chapter, a design example of a bi-directional DC/DC converter with the proposed half-bridges in Chapter 4 is performed and discussed.

5.1 Design Specifications for Bi-Directional DC/DC Converter

Bi-directional DC/DC converters are used for interconnecting two DC terminals where power flow capability is required in both ways. These converters are preferred to be in low volume for high power density applications such as the regulator which connects the battery and motor driver input in an electric vehicle. Fig. 5.1 shows the mind map of a design protocol where "High Power Density" is taken as design input. The converter size is mostly dominated by passive components [61] which can be reduced by increasing switching frequency. However, the high switching frequency results in high switching losses on switching components, especially for high power applications. Soft switching is a method to eliminate switching losses and can be applied to a Buck / Boost type DC/DC converter easily by quasi-square wave zero voltage switching (QSW ZVS). Even though QSW ZVS is an easy way to achieve soft switching, it suffers from high current ripple on inductors which mainly increases the stress on

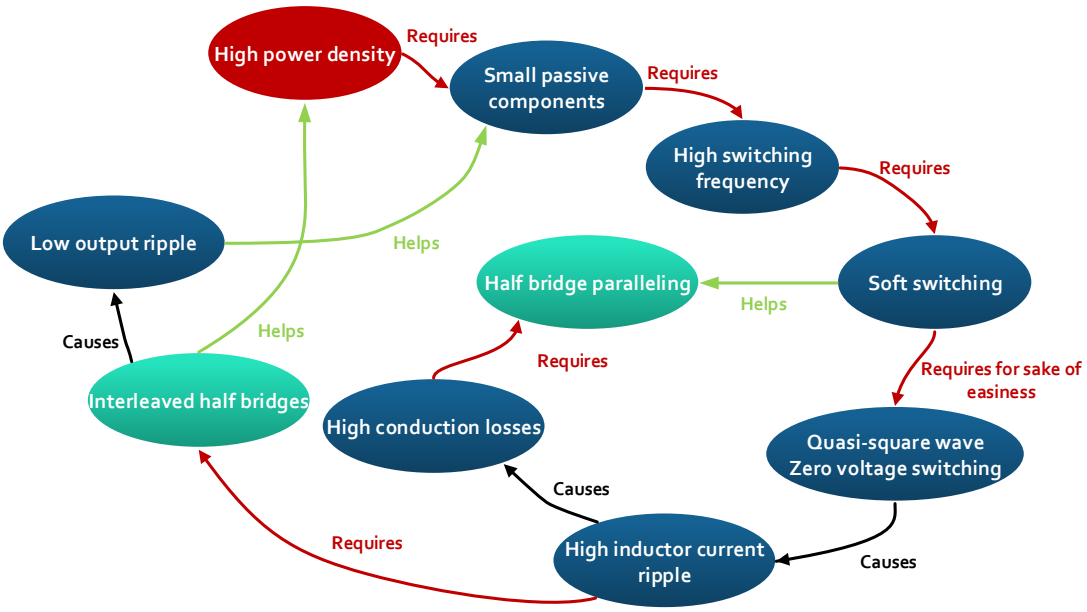


Figure 5.1: Logic diagram of the design of a bi-directional non-isolated DC/DC converter

output filter capacitor and on transistors by causing high conduction losses. Thanks to device paralleling, conduction losses can be shared among parallel-connected transistors and it reduces the conduction loss per switch. Moreover, soft-switching makes device paralleling easy by smoothing switching transitions. The stress on the output filter capacitors can be handled by interleaving half-bridges which significantly shrinks the ripple current flowing through filter capacitors. As a result, the passive components in small size can be used to filter output voltage.

In the lights of these design steps, a bi-directional DC/DC converter scheme is presented in Fig. 5.2 where two ports are denoted as A and B. The power flow from A to B gives the buck operation whereas B to A gives the boost operation.

5.1.1 Achieving Soft-switching by Quasi-square Wave Zero Voltage Switching

Quasi-square wave zero voltage switching (QSW ZVS) is an easy way to achieve zero voltage soft switching (ZVS) in buck/boost type DC/DC converters since it does not require any extra component. The ZVS is accomplished by inductive switching instead of capacitive switching. In capacitive switching, the transistor which is sup-

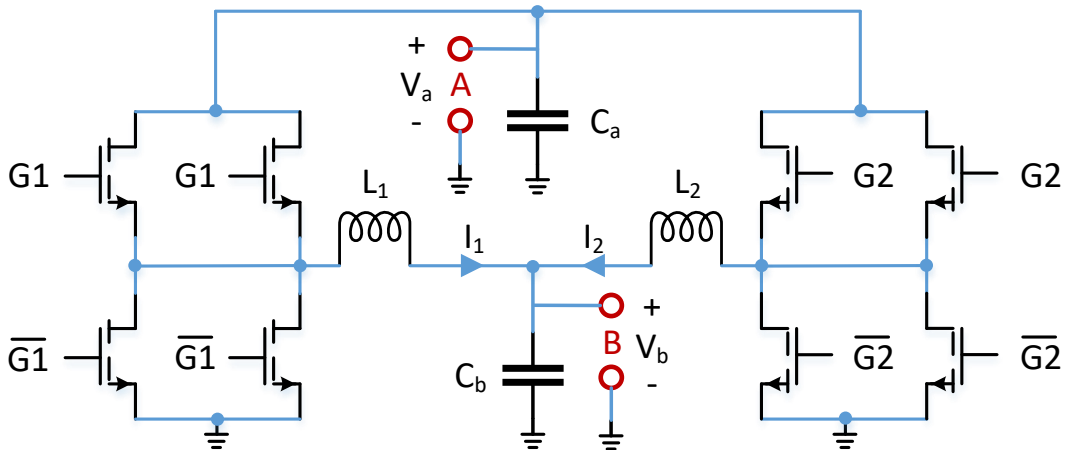


Figure 5.2: Bi-directional DC/DC converter scheme where A and B ports can be configured as input or output

posed to be turned on in the next cycle stays as charged to the DC link voltage level while it is OFF. Therefore, whenever it gets in conduction, the voltage on the output capacitance of the transistor has to be discharged which causes the switching energy dissipation and overshoot on transistor current. However, in inductive switching, the voltage on the output capacitor of the transistor is discharged in dead-time by the load current and the transistor gets in conduction with zero voltage on itself. As a result, the energy is not dissipated during the switching transition.

An example is illustrated in Fig. 5.3 on a buck converter where the inductor current ripple is more than twice of output current; therefore, it goes below zero. Four moments are marked on inductor current in Fig. 5.4 where (1) is the charging moment, (2) is the moment when Q_T turns off and Q_B turns on, (3) is the discharging moment and lastly (4) is the moment when Q_B turns off and Q_T turns on.

As shown in Fig 5.4(a), the inductor is charged with the current flowing through the channel of the high side switch. At the moment (2), high side transistor (Q_T) turns-off and Q_B turns on after a certain dead-time where both of the switches are OFF. During this dead time, the inductor current splits up into two where one part of the inductor current charges the output capacitance (C_{OSS}) of high side switch and other pats discharges the (C_{OSS}) of the low side switch. Then, low side switch is turned-on and inductor current starts freewheeling through the channel of the low side switch

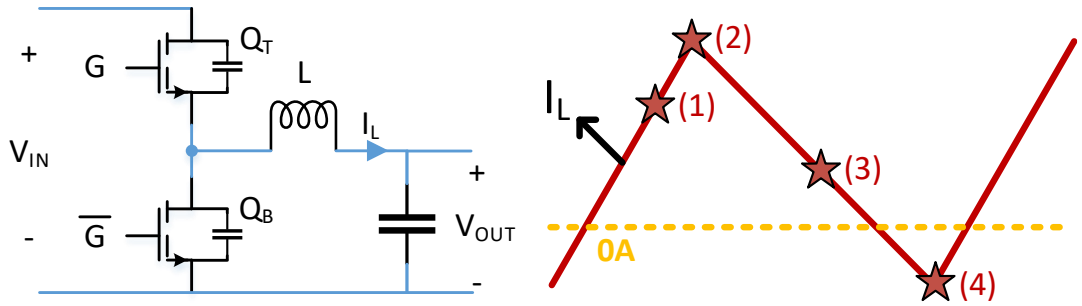


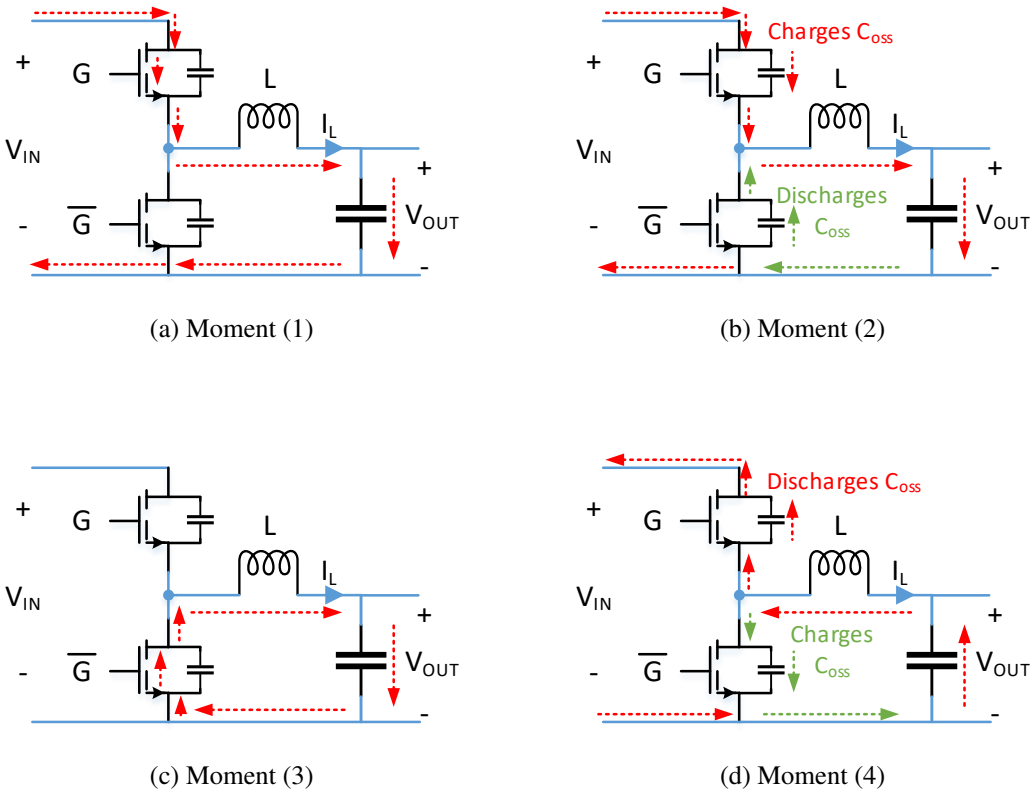
Figure 5.3: Sample moments of quasi-square wave zero voltage switching showing switching characteristic for buck mode operation

as given in Fig 5.4(c). In comparison to continuous conduction mode, the inductor current goes below zero in quasi-square wave zero voltage switching. Therefore, when the low side switch is turned-off as presented in Fig 5.4(d), the inductor current charges the (C_{OSS}) of low side switch and discharges the (C_{OSS}) of high side switch in the dead-time. Even though soft-switching can be achieved easily by QSW ZVS, the inductor current ripple needs to be at least twice of average output current which requires a careful inductor design for high-frequency high-power applications.

Since the inductor current charges and discharges the output capacitance of GaN HEMTs, the required dead time and negative current can be calculated. Since a parallel switching operation is applied in this design, the resonant current has to charge or discharge the output capacitances of both transistor in parallel-connection. Therefore, the total output capacitance needs to be considered as double of the output capacitance of a single transistor for high side and low side. The actual value of the output capacitance is characterized in Chapter 2. According to the experimental results, the equivalent output capacitance of the device at 0 to 400 V or vice versa transition can be calculated by using the energy as described in (5.1). The output capacitance is found as 108 pF which is given as 100 pF in the datasheet [4].

$$E_{oss} = \frac{1}{2} C_{oss} V_{dc}^2 \tag{5.1}$$

The inductor current which flows in a negative direction at that moment charges two GaN HEMTs and discharges two GaN HEMTs as presented in Fig. 5.5. According to the principle of conservation of charge, the required current or duration can be cal-



(a) Moment (1)

(b) Moment (2)

(c) Moment (3)

(d) Moment (4)

Figure 5.4: Steps of quasi-square wave zero voltage switching defined in Fig. 5.3 for buck mode operation

culated as shown in (5.2). For a configuration that operates under 400V DC bias and where 4 A of negative current flows, a dead time of 43 ns is required as a minimum to achieve zero voltage switching. Considering the gate charge and discharge duration, 100 ns of dead time would be suitable and safe for this design.

$$t_{dead}\hat{I}_{L,neg} = 4C_{oss}V_{dc} \tag{5.2}$$

The parallel-connected bridge structure is tested on a simulation platform with 100 ns of a dead-time period. The results show that, high side switch, i.e. the control switch for buck mode, turns-on with zero voltage switching as shown in Fig. 5.6.

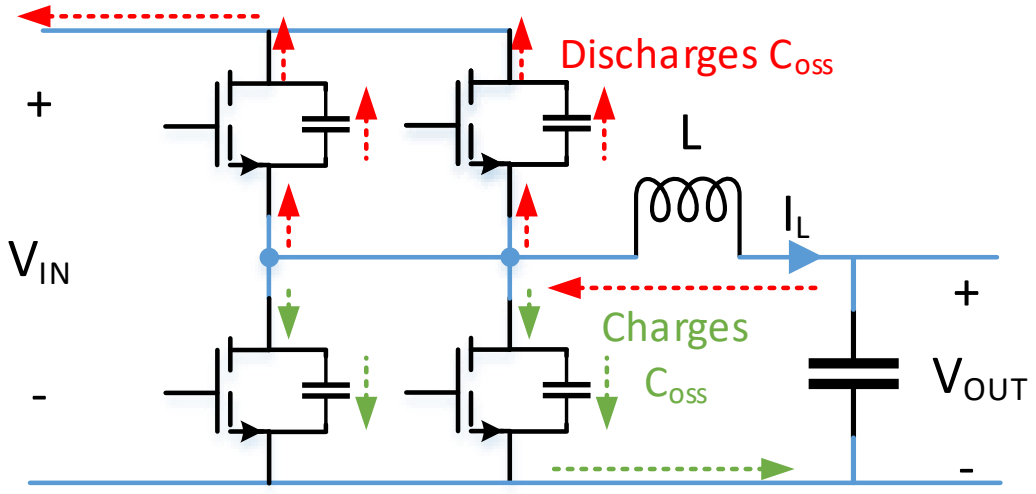


Figure 5.5: Achieving soft switching at turn-on with parallel connected devices

5.1.2 Interleaving

As discussed before, quasi-square wave zero voltage switching suffers from high current ripple. Behind the thermal stresses caused by the current ripple, it causes output voltage swing as well unless the filter capacitors are capable of filtering. Instead of applying all current ripple to the output filter capacitors, interleaving the multiple numbers of bridges could decrease or eliminate the ripple. Moreover, the thermal stress per bridge decreases as well for the same operating point.

The nominal operating conditions are given in Table 5.1. Based on these operating conditions, the number of the interleaved bridge is selected with theoretical and practical reasons. Theoretically, the number of interleaved bridges is evaluated and compared as shown in Table 5.2. Since buck and boost modes operate with almost complementary duty cycles, minimum ripple is obtained for the same number of bridges. Interleaving three bridges is the most suitable option for buck and boost modes in terms of ripple cancellation. Moreover, the transferred power per bridge decreases with an increasing number of bridges. That ratio could have been kept constant by taking the chance of increased output power. However, the available electrical loads and power supply limitations are the practical reasons for keeping output power constant. By keeping the output power constant, the increased number of bridges decreases the utilization of filter inductors and switches. As a result, interleaving two bridge seems

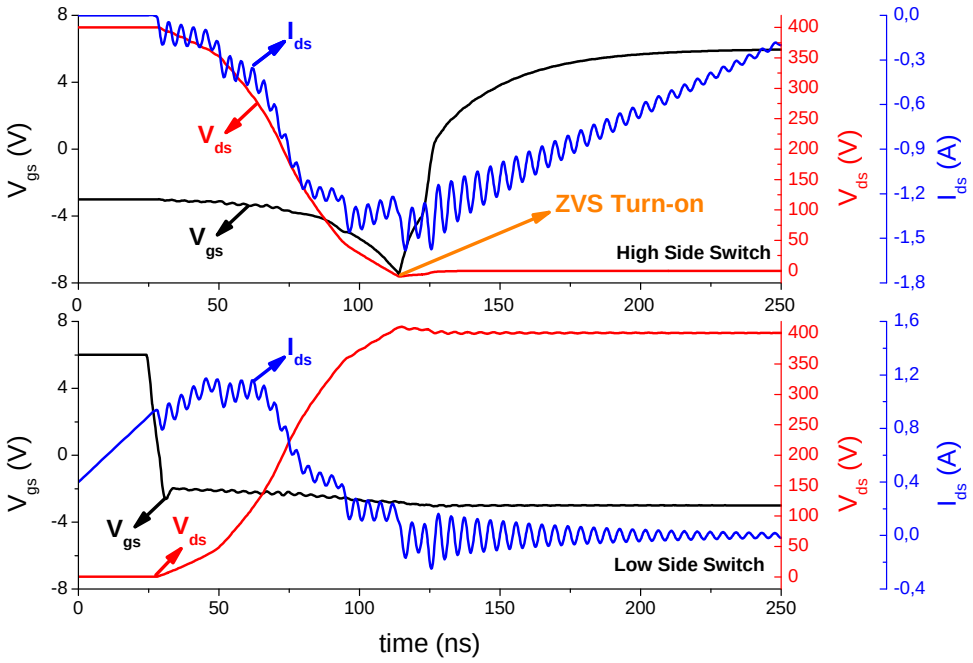


Figure 5.6: Simulation results showing zero voltage switching for high side switch at turn-on

Table 5.1: Nominal operating conditions for buck and boost modes

	Buck Mode	Boost Mode
Input Voltage	400 V	270 V
Output Voltage	270 V	400 V
Duty Cycle	0.675	0.323
Output Current	20 A	13.5 A
Output Power	5.4 kW	

Table 5.2: Comparison of the effects of interleaved bridge number

	Buck Mode	Boost Mode			
Number of bridges	$\frac{\Delta I_{cap}}{\Delta I_L}$		kW/bridge	$\frac{\Delta I_L}{\bar{I_L}}$	Color Code
1	1	1	5.4	2.4	Best
2	0.515	0.521	2.7	2.8	Better
3	0.037	0.045	1.8	3.2	Not Bad
4	0.235	0.228	1.35	3.6	Bad
5	0.21	0.209	1.08	4	Worse

Table 5.3: Inductor specifications obtained by simulation results

Inductance	6.8 μH
Frequency	450 kHz
Average Current	10 A
Ripple Current	28 A_{pp}

to be the most advantageous case for handling the ripple while maximizing the power density.

5.1.3 Inductor Design

The inductor design is one of the most critical steps for the QSW ZVS converter because the increased current ripple can saturate the magnetic core or cause lots of heat dissipation on the inductor. The total inductor loss can be estimated by summing winding losses and core losses as shown in (5.3). Nevertheless, the winding losses can be split into two parts as the DC losses and AC losses. For an inductor with the multiple numbers of layers and thick wires, AC loss dominates due to the eddy effects.

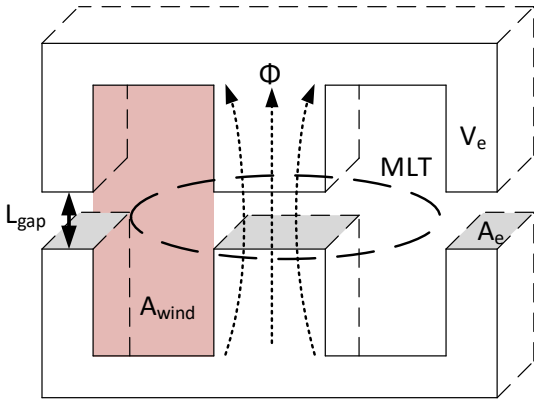


Figure 5.7: Definitions of E shaped magnetic core

Therefore, the thickness of the wire should be selected by taking the skin depth into account. In this design, aimed switching frequency is 450 kHz and inductor should carry 10 Amps on average with 28 Amps peak-to-peak ripple as given in Table 5.3. The skin depth for 450 kHz is 97.2 μm, so a Litz wire needs to be used to handle the ripple. A Litz wire with 400 strands of 80 μm of thickness is chosen.

$$P_{ind} = P_w + P_c \tag{5.3}$$

Off the shelf magnetic gapped E cores on the shelf are not suitable for this application. Therefore, a gapless E core is used and the air gap is adjusted with a few piece of isolation papers as shown in Fig. 5.7. Basically ignoring the reluctance of E core, the total reluctance of the flux path can be formulated as given in (5.4). The turn number can be written down with the calculated reluctance and desired inductance as presented in (5.5). With the turn number and reluctance, the flux density can be calculated as given in (5.6) and (5.7) to check if the magnetic core saturates (5.8). Moreover, the AC flux density (B_{ac}) is required to estimate core loss as well.

$$\Re = \frac{2L_{gap}}{\mu_o A_e} \tag{5.4}$$

$$N \simeq \sqrt{L * \Re} \tag{5.5}$$

$$B_{dc} = \frac{NI_{avg}\mu_o}{2L_{gap}} \tag{5.6}$$

$$B_{ac} = \frac{N\Delta I\mu_o}{4L_{gap}} \tag{5.7}$$

$$B_{peak} = B_{dc} + B_{ac} \tag{5.8}$$

Another important measure for the inductor is the power loss caused by the current. For this purpose, DC resistance of the winding and AC resistance should be calculated. The total copper area of Litz wire is 2 mm^2. Therefore, the resistance of the wire can be found as given in (5.9) where MLT stands for mean length of a turn. More importantly, the AC resistance should be determined with respect to DC resistance using Dowell curves. The winding layer has to be kept as small as possible. Therefore, for the first core selection step, AC resistance is taken as 1.5 times of DC resistance.

$$R_{dc} = \frac{\rho N(MLT)}{A_{wire}} \tag{5.9}$$

$$P_{dc} = I_{avg}^2 R_{dc} \tag{5.10}$$

$$P_{ac} = I_{rms}^2 R_{ac} \tag{5.11}$$

$$P_{core} = P_{sp}(B_{ac}, f)V_e \tag{5.12}$$

As a result, power losses of a magnetic core can be calculated as shown in (5.10), (5.11) and (5.12). Core loss is calculated with the given specific power loss in the magnetic core datasheet. The specific power constant changes with respect to AC magnetic flux density and frequency. The total power loss is compared for different magnetic cores and presented in Fig. 5.8. Even though, the magnetic core

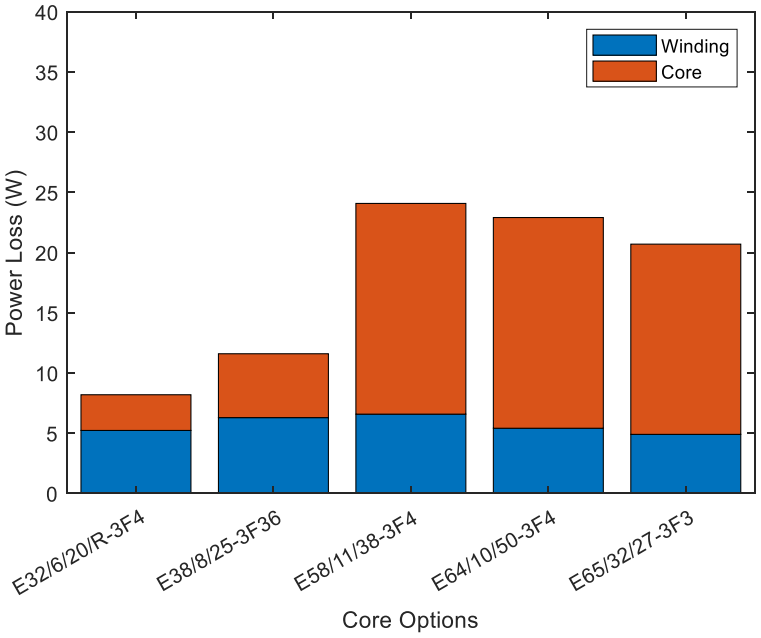


Figure 5.8: Loss comparison of different magnetic cores

E32/6/20/R-3F4 [62] seems advantageous in terms of power losses, its fill factor is higher than others as shown in Fig. 5.9. The magnetic core E38/8/25-3F36 [63] has less than 20% fill factor and suitable for paralleling two Litz wires so that the winding loss could be halved. The final loss of E38/8/25-3F36 can be reduced down to 8.5 W. Also, its dimensions are slightly higher than E32/6/20/R-3F which gives a larger cooling surface area.

The wounded magnetic core is shown in Fig. 5.10(a) where two E cores will be placed on top of each other and wires will be paralleled. The final view of the inductor is presented in Fig. 5.10(b).

5.1.4 Filter Capacitor Selection

On the one hand, interleaving half-bridges reduce the current ripple for the output capacitor. On the other hand, the frequency of filter capacitor current increases as much as switching frequency times the number of interleaved bridges. Therefore, for two interleaved bridges, the filter capacitor carries the current with double switching frequency. The simulation result presented in Fig. 5.11 shows the inductor currents

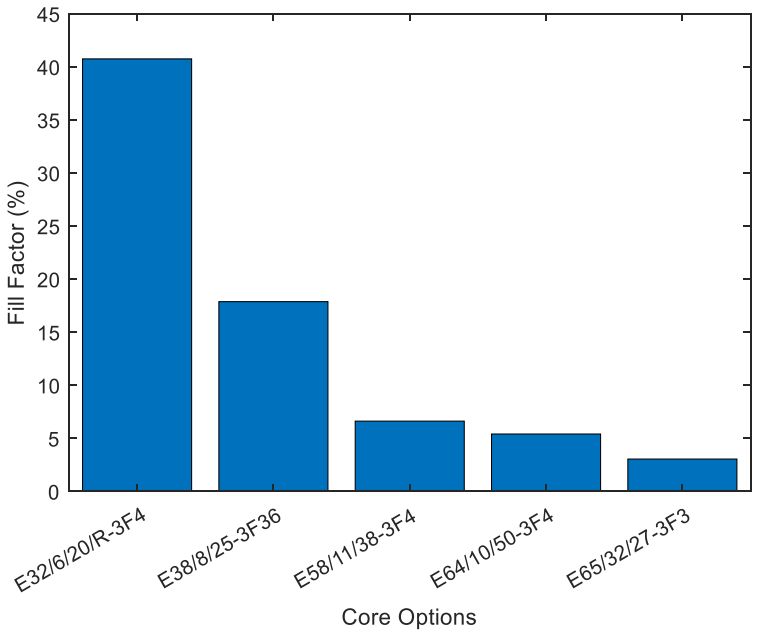


Figure 5.9: Fill factor comparison of different magnetic cores

(a) Inductor winding

(b) Inductor

Figure 5.10: View of inductor

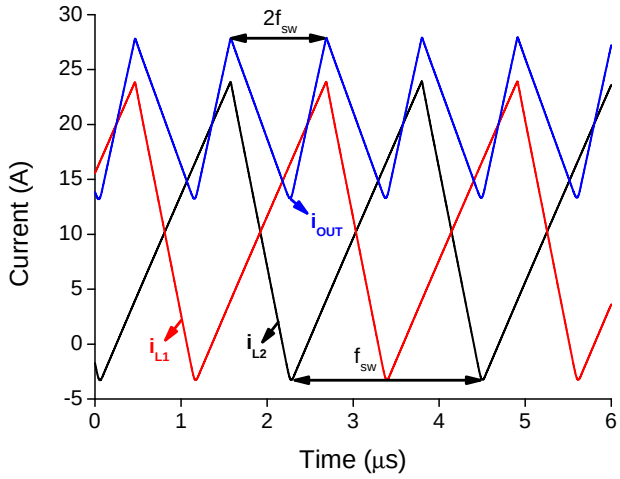


Figure 5.11: Interleaved inductor currents and output current

and the output current for rated buck mode operation. According to the simulation results, the amplitude of the ripple current is almost halved and the frequency is the double of switching frequency, 900 kHz. For 1% output voltage ripple, the filter capacitor should be higher than 690 nF according to (5.13). This calculation is valid only for an ideal capacitor and ideal connections which is not the case for a practical application. Ideally, the output voltage does not swing more than calculated as long as the ripple on the output current passes through the filter capacitor. However, capacitors are not ideal and have parasitic inductances and resistances. Therefore, the frequency response of the filter capacitor gets important since it should carry a considerably high amplitude of ripple current at 900 kHz. Moreover, the dissipation factor has to be low enough to keep capacitors thermally safe.

$$C = \frac{\Delta I}{8\Delta V(2f_{sw})} \tag{5.13}$$

The RMS of the current to be carried by the capacitors is 7.8 A at 900 kHz. In order to filter out this current, two surface mount design (SMD) film capacitors, LDEPH32 20KA5N00 [64], and one through-hole (TH) film capacitor, BFC238320684 [65], are used. Fig. 5.12 and Fig. 5.13 shows the current-carrying capability of SMD and TH film capacitors, respectively. The total capacitance is 1120 nF and the current range goes up to 23 A which is higher than the required values. Both capacitors are rated as

630 V as maximum.

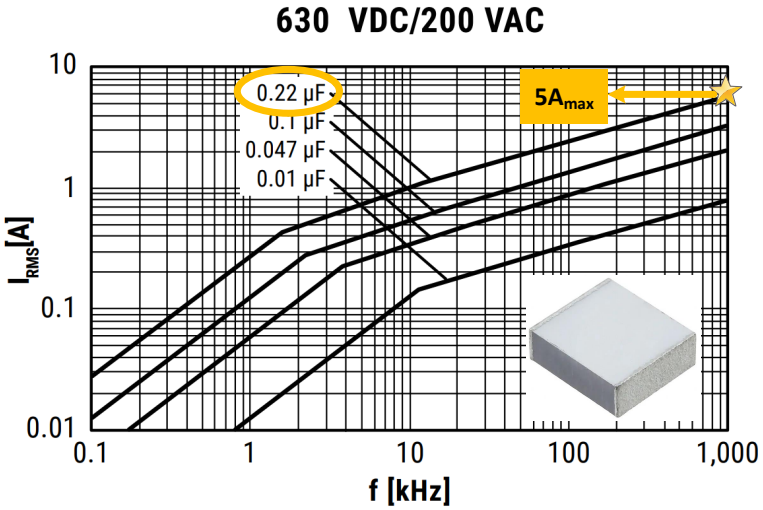


Figure 5.12: Maximum current carrying capability of SMD film capacitor, LDEPH3220KA5N00

5.2 Experiments and Results

The bi-directional DC/DC converter is physically implemented and tested under full load for both buck and boost modes with the presented experimental setup in Fig. 5.14. During the experiments, all waveforms are recorded by a digital oscilloscope, LeCroy Waverunner 44xi, and the current waveforms are measured by a current probe, TCP305A. Resistive banks are connected in parallel as load. Input and output powers are measured by watt-meters.

The converter is able to operate at full load and it does not require any extra cooling to overcome thermal loading as will be discussed in Section 5.2.1. Converter dimensions are 7.5 cm, 11 cm, 12.5 cm as shown in Fig. 5.15 which results in 5.24 kW/l power density at full load.

The experiments are organized as the following. Section 5.2.1 gives the thermal tests where a different level of thermal stresses are applied to inductors and heat sinks of GaN HEMTs. In Section 5.2.2 and Section 5.2.3, the operation tests are performed for buck mode and boost mode under different loading conditions.

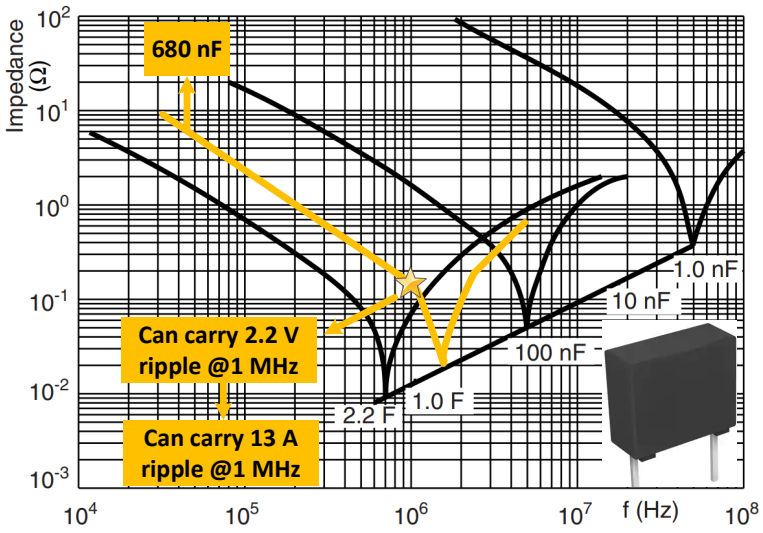


Figure 5.13: Maximum current carrying capability of through hole film capacitor, BFC238320684

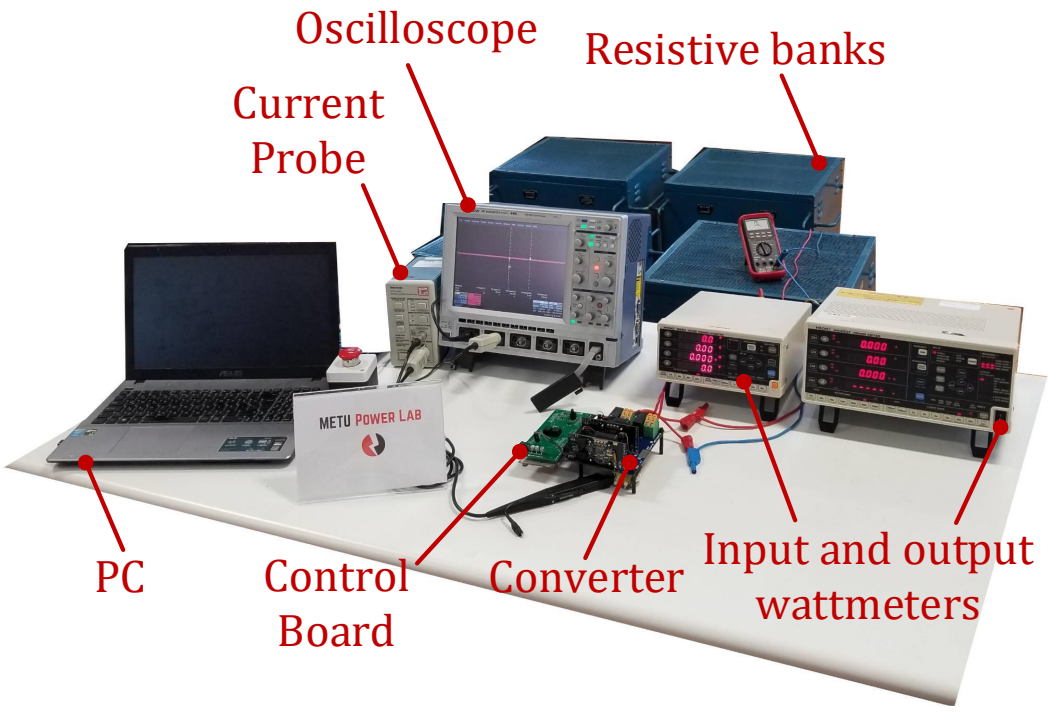


Figure 5.14: Experimental setup of the bi-directional DC/DC converter

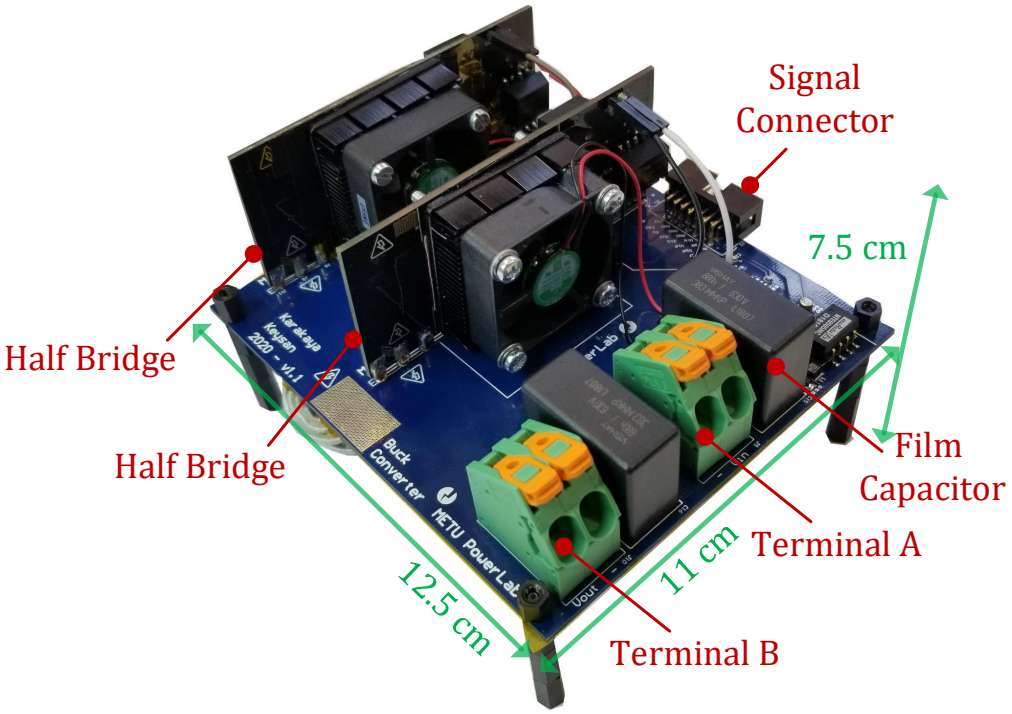


Figure 5.15: Bi-directional DC/DC Converter with 1.03 l volume

5.2.1 Thermal Tests

The thermal resistance of the magnetic core of the inductors is not presented clearly in the datasheet. Therefore, the thermal design has to be verified before applying full load. The thermal stresses of the inductors are dominated by the AC winding losses and the core losses which both are got affected by the switching frequency. In order to see the effect of switching frequency, the rated ripple amplitude of the current is applied to the inductors to see the cooling performance.

Thermal measurement points are shown in Fig. 5.16. In each rectangle, the hottest point is recorded for each switching frequency. The input voltage and duty cycle are adjusted so that always the same current flows through the inductors with different frequencies. The operating frequency is changed from 150 kHz to 450 kHz with 50 kHz steps and the current waveform recorded by the oscilloscope is shown in Fig. 5.17 for the minimum and the maximum frequencies. The resulting temperatures are shown in Fig. 5.18 where the maximum temperature increases up to 122 °C at windings and the ambient temperature is 25 °C. Note that, in this study, all thermal

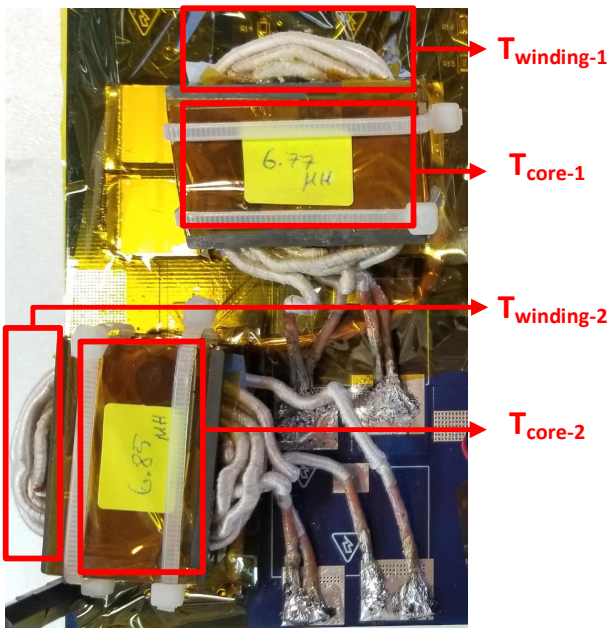


Figure 5.16: Thermal measurement points over the inductors

results are measured after 30 minutes of operation.

Moreover, it is important to see the effects of the current ripple and average separately to figure out the main reason behind the heating of passive components or GaN HEMTs. For this purpose, two test sets are performed. On the one hand, the average current of the inductor current is changed while the ripple magnitude of the current stays as the same and on the other hand, the average of the inductor current is kept constant while the ripple changes. The results of these two experiment sets are shown below in Fig. 5.19 and Fig. 5.20. The temperature is recorded for five different components, the inductor winding and the core, heat sink of GaN HEMTs and input capacitors. These components are the ones subject to heating in the experiments. Fig. 5.19 shows that the effect of the change in the average current is limited and does not affect the temperatures of the components much more. However, the current ripple is decisive over the heating as given in Fig. 5.20.

In order to guarantee safe operation for passive components under full load, a fan is placed, without reducing the power density, to overcome any harmful heating. This configuration is presented in Fig. 5.21. Table 5.4 gives how the fan affects the temperatures of the components. As expected, it significantly reduces the temperature of

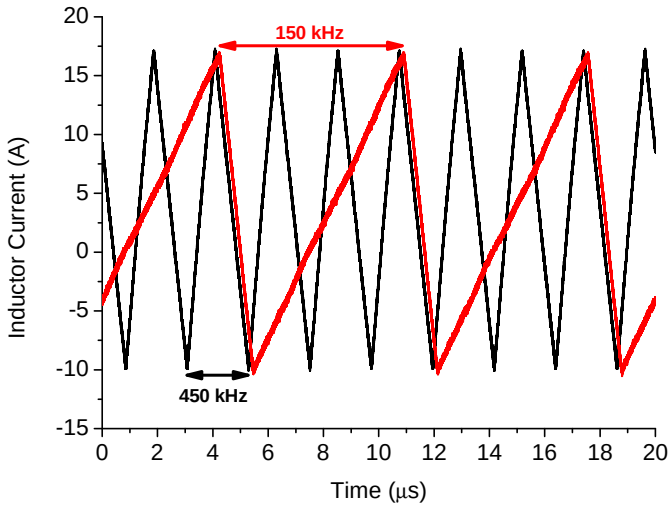


Figure 5.17: Applied currents on the inductors for thermal tests

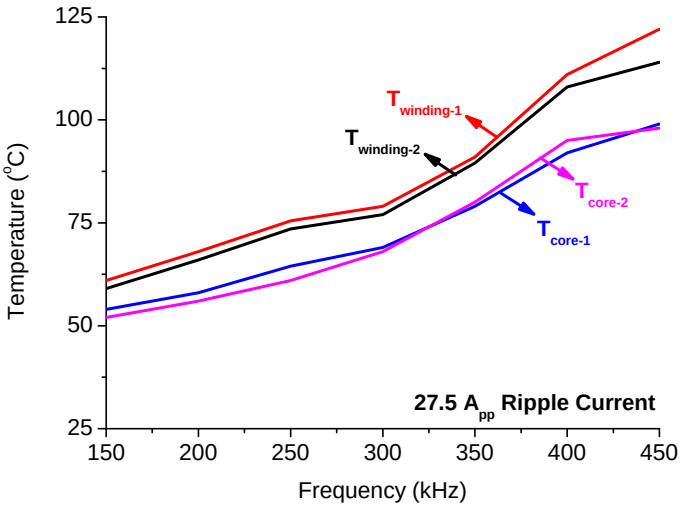


Figure 5.18: Steady-state temperature results of inductors for varying switching frequency

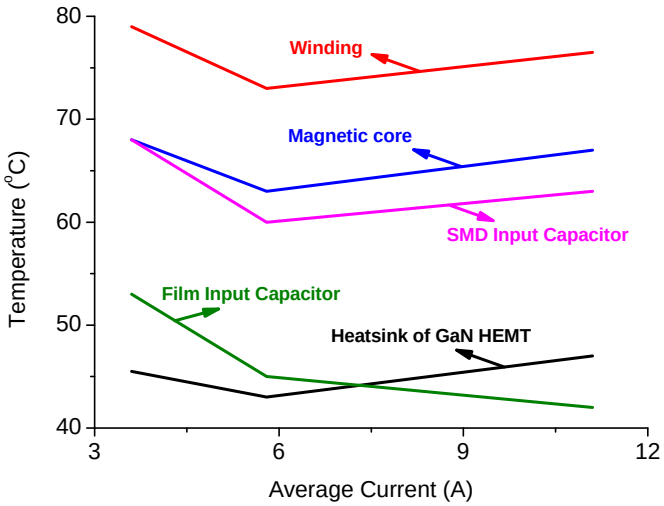


Figure 5.19: The temperatures of different components under constant ripple (20A, 450 kHz), varying average current over inductor

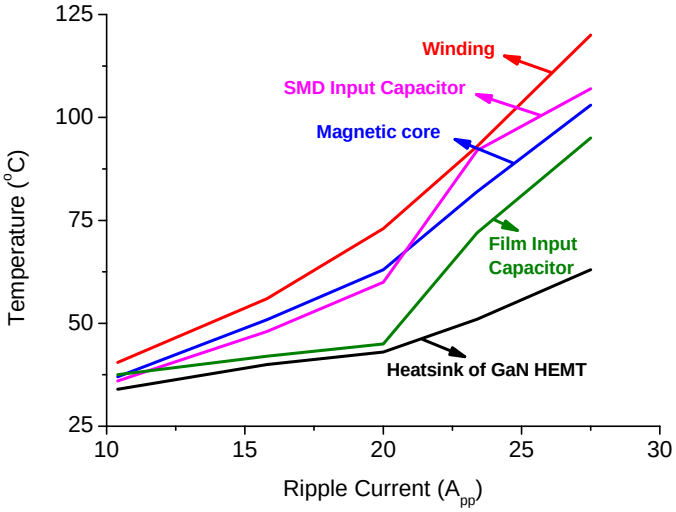


Figure 5.20: The temperatures of different components under constant average (5.8A), varying ripple current magnitude (450 kHz) over inductor

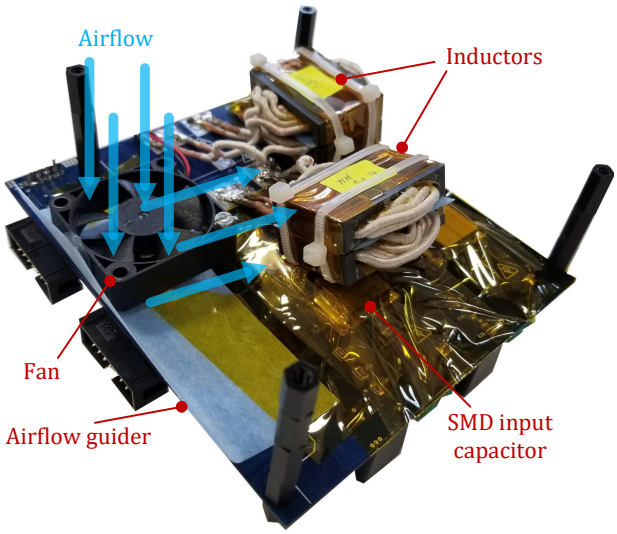


Figure 5.21: The view of the converter with the fan placed for cooling passive components

the inductor and SMD input capacitors which are on the same side of the PCB. Its effect on the film input capacitor and GaN HEMT heat sink is limited since they are on different sides of the PCB.

Lastly, another important point is to estimate the junction temperature of GaN HEMTs for different operating points of the bi-directional converter. The important thing is to scale losses with respect to the inductor current. Note that, as a result of ZVS switching the voltage level does not affect the losses. As discussed before, the ripple current is more dominant on the losses rather than the average. However, the actual loss source is the total effective value of the current on the inductor. Based on the experimental results, it is deduced that the power losses of the GaN HEMTs on a half-bridge are proportional to the square sum of average current and ripple current as given in (5.14).

$$P_{bridge} \propto I_{L-DC}^2 + (\frac{I_{L-PP}}{\sqrt{3}})^2 \tag{5.14}$$

Now, it is possible to scale the temperature rise on the heat sink based on a reference measurement. The heat sink temperature is recorded as 43 °C under 5.8 A average and 20 A_{pp} ripple current. The final formula is given in (5.15) where the temperature

Table 5.4: Effect of the fan for the operation with 3 A average and 28.3 A ripple current over the inductor at 25 °C of ambient temperature

	Without fan	With fan
Winding	131 °C	86 °C
Magnetic core	119 °C	79 °C
SMD input capacitor	112 °C	60 °C
Film input capacitor	49.5 °C	44 °C
GaN HEMT heat sink	59 °C	57.5 °C

of the heat sink is found for an operating point using a reference measurement.

$$T_{HS-op} = (T_{HS-ref} - T_{amb}) \frac{I_{L-DC-op}^2 + (\frac{I_{L-PP-op}}{\sqrt{3}})^2}{I_{L-DC-ref}^2 + (\frac{I_{L-PP-ref}}{\sqrt{3}})^2} + T_{amb} \tag{5.15}$$

Lastly, the junction temperature can be estimated with the same method. For this purpose, the losses extracted from the simulation results are taken as the reference. Based on the simulation results, the losses of the GaN HEMTs over a half-bridge are 18.7 W where the average and ripple current of the inductors are 20 A and 27.5 A_{pp}, respectively. The thermal design of the half-bridge boards was discussed in Section 4.3 in detail. The resulting equation is presented in (5.16). The estimated temperatures will be compared with the actual measurements in the following steps.

$$T_{j-op} = P_{ref} \frac{I_{L-DC-op}^2 + (\frac{I_{L-PP-op}}{\sqrt{3}})^2}{I_{L-DC-ref}^2 + (\frac{I_{L-PP-ref}}{\sqrt{3}})^2} R_{j-hs} + T_{HS-op} \tag{5.16}$$

5.2.2 Buck Mode

In buck mode tests, the input voltage is set to 400 V, and the applied duty cycle is kept constant to have the same output voltage. Note that, since this converter applies

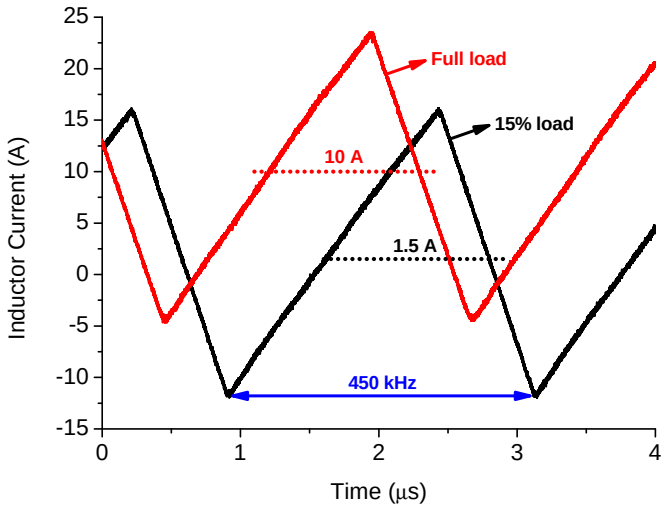


Figure 5.22: Inductor current for 15% load and full load of buck operation

synchronous switching, there is no discontinuous conduction mode operation for any load, so the volt-second balance equation is always the same as presented in (5.17). Therefore, the input to output gain is always the same as well as given in (5.18).

$$(V_{in} - V_{out})D + (-V_{out})(1 - D) = 0 \tag{5.17}$$

$$\frac{V_{out}}{V_{in}} = D \tag{5.18}$$

During the tests, the load is increased by 15% in each step. Measured inductor current waveform is presented in Fig. 5.22 for the minimum and maximum loading conditions. In each step, the critical temperature points are recorded so that the thermal performance could be verified under rated operating conditions. The change in the temperature is shown in Fig. 5.23 for a varying load current range. The estimated heat sink and junction temperature are also plotted. As shown, there is a good match between the estimated and actual heat sink temperatures. Moreover, it is estimated that the junction temperature rises up to 131 °C under full load.

The output voltage ripple is measured and shown in Fig. 5.24 for full load condition. Nevertheless, the output voltage ripple gets affected by the duty cycle, frequency, and

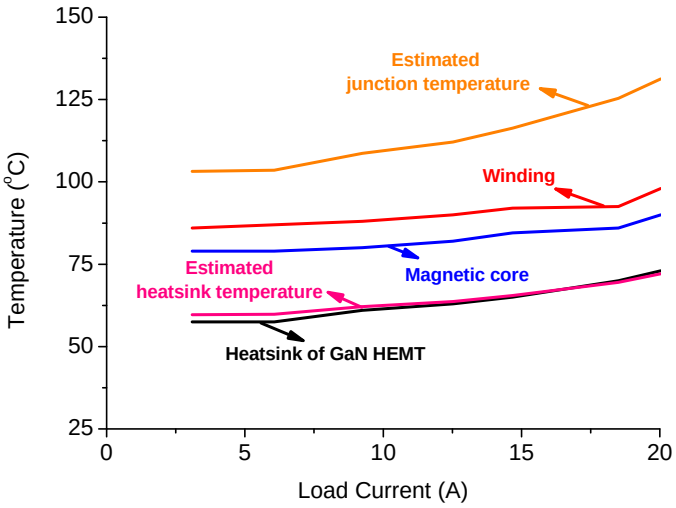


Figure 5.23: Temperature change of GaN HEMTs and inductors for varying loading conditions of buck mode operation

input voltage. Since these three parameters are the same for all load range, the output voltage ripple is constant over the load current. According to the experimental results, the output voltage ripple swings as 2.3 V which is less than 1% of the output voltage.

Finally, the efficiency curve is obtained for the buck mode operation and presented in Fig. 5.25. The results show that 97.7% efficiency is reached for the full load and 97.9% efficiency is obtained as the peak. Note that, the efficiency curve is obtained based on the electrical measurements and subject to an error margin of measurement tools. A better efficiency curve would be obtained with a calorimeter [66].

5.2.3 Boost Mode

In the boost mode tests, the output voltage is set to 400 V, and the input voltage is kept constant at 270 V. Again due to synchronous switching, the converter does not operate in discontinuous conduction mode. Therefore, the volt-second equation of the converter turns into (5.19), so the gain is as in (5.20).

$$V_{in}D + (V_{in} - V_{out})(1 - D) = 0 \tag{5.19}$$

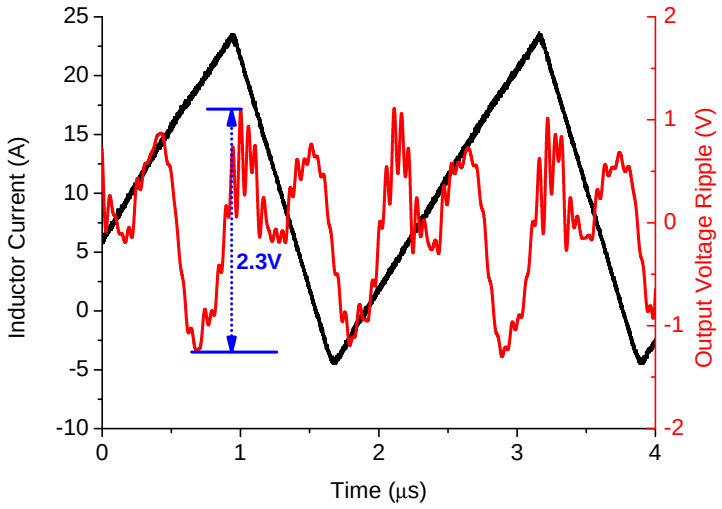


Figure 5.24: Output voltage ripple under rated load conditions

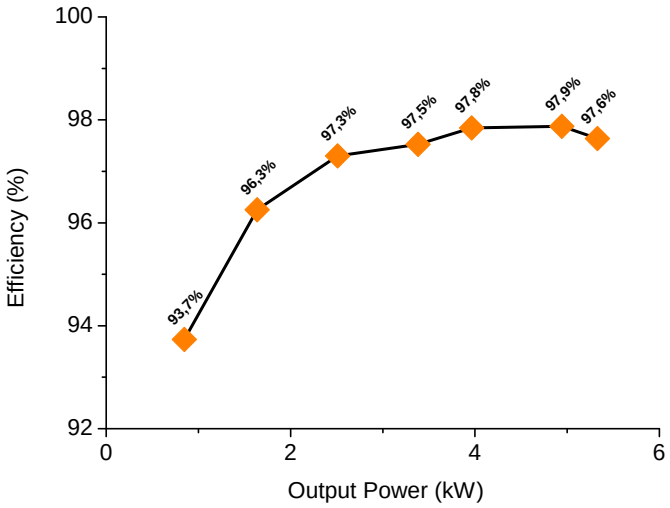


Figure 5.25: Efficiency curve of buck mode operation based on electrical measurements

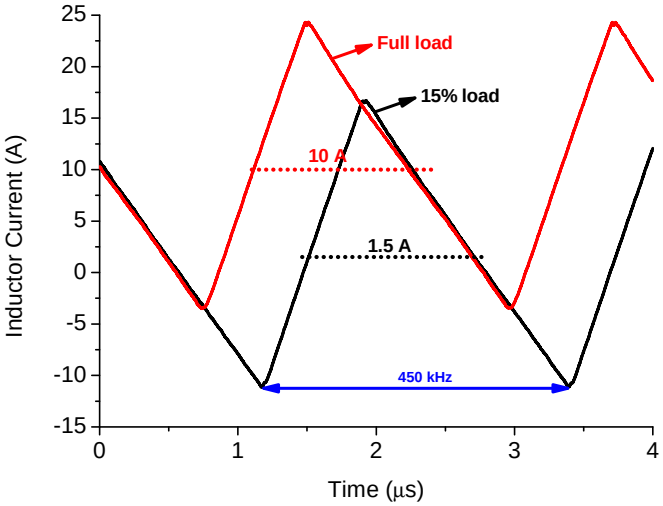


Figure 5.26: Inductor current for 15% load and full load of boost operation

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \tag{5.20}$$

Figure 5.26 gives the inductor currents for full load and 15% load. During the tests, the load is increased by 15% steps. Under full load condition, the estimated junction temperature goes up to 137 °C as shown in Fig. 5.27. Considering the maximum junction temperature of GaN HEMTs is 150 °C, the temperature limit of the GaN HEMT is almost achieved. In order to estimate junction temperature, equations (5.15) and (5.16) are used with calibrating according to the simulation results of boost mode. Simulation results give 19.1 W total loss for GaN HEMTs on a half-bridge under full load condition, 400 V, 5.4 kW output in boost configuration.

Moreover, in Fig. 5.28, the thermal view of the converter under full load is presented for boost mode. Image A shows the temperature increase on the PCB trace which is connected to the drain of the high side switch. The heat sink temperatures are shown on image B where one of the half-bridge heats up much more than others due to hot airflow caused by cool half-bridge. Lastly, thermal views of the inductors are shown in image C.

In the boost mode, experimental results show that the output voltage swings with 3.9 peak to peak amplitude under full load. Therefore, the output ripple is less than 1%

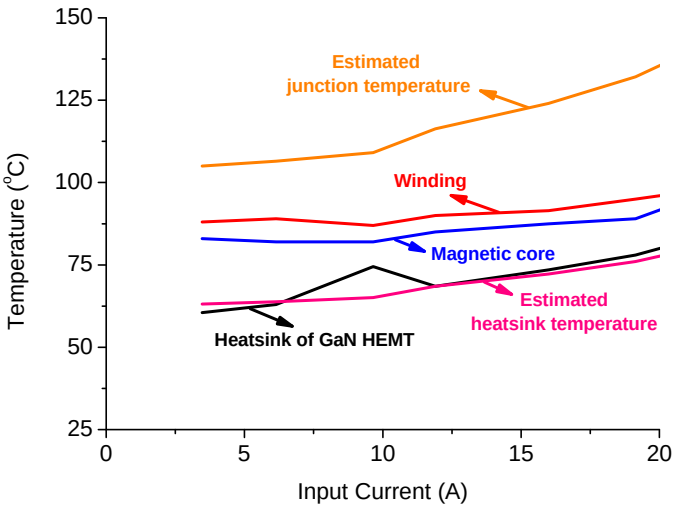


Figure 5.27: Temperature change of GaN HEMTs and inductors for varying input current of boost mode operation

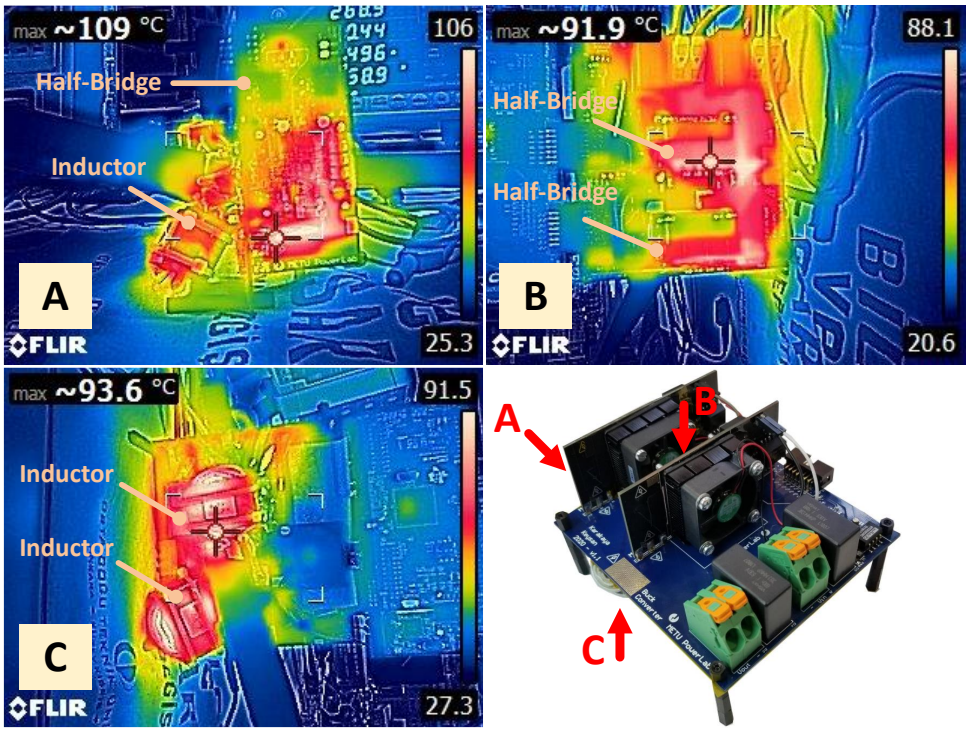


Figure 5.28: Thermal camera view of the converter under full load for the boost mode

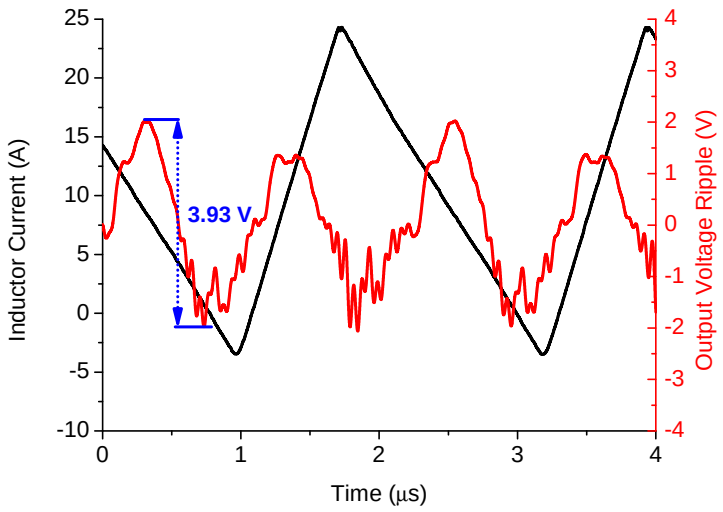


Figure 5.29: Output voltage ripple under rated load conditions

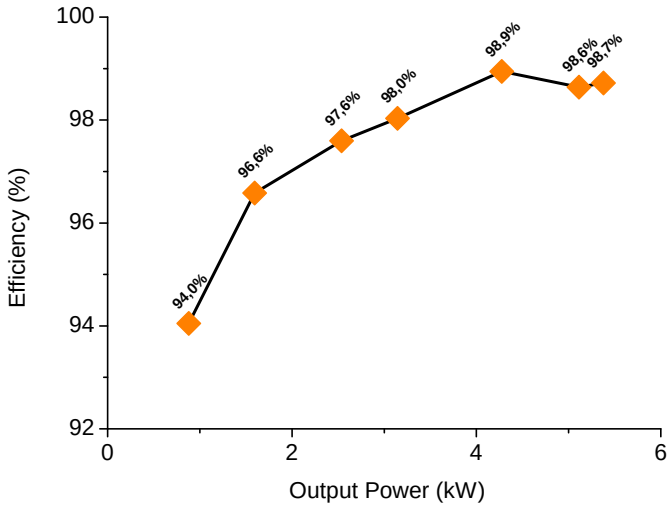


Figure 5.30: Efficiency curve of boost mode operation based on electrical measurements

as shown in Fig. 5.29. The voltage ripple is not affected by the load current since the duty cycle is kept constant for the whole load range.

Lastly, the efficiency of the converter is measured as 98.7% at full load in the boost mode. The efficiency curve of the converter is given in Fig. 5.30.

In conclusion, this chapter gives an example design with the proposed half-bridge boards. A bi-directional DC/DC converter application is selected where the power rating goes up to 5.4 kW and switching frequency is 450 kHz. The converter utilizes a quasi-square wave zero voltage switching to eliminate switching losses. As a requirement of QSW ZVS, the filter inductance is kept low so that the inductor current can flow in both directions in a switching cycle. Therefore, an inductor design is performed where the ripple current is set as 28 A in magnitude with 450 kHz frequency. Moreover, interleaving is applied to cancel ripple current and reduce the stress over output capacitors. The converter is tested in buck and boost configurations under rated power. Thermal results are presented and an efficiency curve is obtained for a wide range of output power. The converter is able to operate at 97.7% and 98.7% efficiencies under full load in buck and boost modes, respectively. As a result, 5.24 kW/l or 85.9 W/in^3 of power density is achieved.

CHAPTER 6

CONCLUSIONS

In this thesis, the GaN HEMTs are studied in a perspective from component to system level. The device parameters are characterized and their effects are investigated on the switching performance. Then, using the characterized device, a half-bridge prototype is designed where device paralleling is applied which requires layout optimization. Additionally, shoot-through type short circuit protection is implemented on the same half-bridge board to increase reliability. Lastly, the designed half-bridges are used in a bi-directional DC/DC converter application to maximize power density.

6.1 Outcomes and Discussions

Firstly, gate charge of a GaN HEMT is characterized by the soft-switching transition. The gate charge might cause unexpected amount of losses for very high-frequency applications like class amplifiers. For this purpose, the gate loss needs to be characterized. This study utilizes three different gate charge values for the loss estimation: the datasheet provided gate charge (6.1 nC), the measured gate charge by the impedance analyzer (4.7 nC), and the gate charge extracted from thermal tests (4.9 nC). According to the experimental results, the gate charge given by the manufacturer deviates more than 25% from the actual gate charge for a soft switching application. A more accurate and easy way is to use an impedance analyzer to reduce the error margin below 5% whereas the actual charge can be figured out by thermal tests. The main reason for the error in manufacturer record is that the gate charge is measured under a hard-switching case.

Another important parameter of GaN HEMTs is the output capacitance, which plays a

significant role over switching losses and switching transitions. A non-linear resonance-based characterization method is utilized and experimentally verified. For this purpose, a printed circuit board is designed where GS66508T GaN HEMT is connected in series with a 150 μH inductance. The drain-source voltage of the transistor is charged up to 550 V and the waveform is recorded by the oscilloscope. The extracted capacitance curve complies with the datasheet curve and the stored energy is in a good match with manufacturer value. This method, without requiring any specific source or tool, is a simple way to characterize the output capacitance of a device that varies with respect to the bias voltage.

Having characterized device parameters, it is important to see how they affect the switching performance of the device. Understanding the effect of the parasitics on turn-on and turn-off characteristics of GaN are important to understand GaN behavior and safe operation. For this purpose, a GaN device, GS66508B, is modeled and the model is verified by comparing simulation results with the datasheet parameters. Then, the channel current and channel voltage, which represent device characteristics better, are investigated on a double pulse test circuit using an accurately modeled GaN device. The simulation results belonging to channel current and voltage waveforms are presented as state-trajectories on the steady-state I_{ds} – V_{ds} graph to discuss characteristics better. Moreover, in order to emphasize and express the unique conduction characteristics of GaN better, important definitions, active/passive turn-on/off, are explained.

Furthermore, the effects of the temperature on the channel trans-conductance and oscillations are studied on state-trajectory plots. It is shown that increasing operation temperature reduces trans-conductance significantly, so the overshoots and damping time of oscillation are decreased for high junction temperature of the device. Additionally, the state-trajectories are shared for different load ratings and it is shown that the transient gate-source voltage is affected by the current whereas the switching speed is not changed as expected. Lastly, the channel voltage and channel current transitions are given on the time axis for different turn-on and turn-off resistances. High gate-driver resistances make the switching period longer, so since the current changes slowly, the overshoots in current and voltage drops decrease.

Even though GaN HEMTs are very attractive devices with their characteristics, the maximum utilization can only be reached with optimized layout design. Non-optimized layout design can easily deteriorate or even block the operation. Therefore, the important points for optimization of the power loop and the gate loop design are investigated and verified by finite-element-analysis results. Three different power loop designs are compared where one of them is the design proposed by the manufacturer. According to FEA results, maximum utilization of bypass capacitors is very important and the power loop inductance can be reduced by 40%. Moreover, the utilization of parallel devices requires much more attention to the layout design. An example design is performed and it is experimentally shown that parallel-connected GaN HEMTs turn-on and turn-off simultaneously based on V_{gs} and V_{ds} waveform records. However, though the layout is optimized, GaN HEMTs can get affected by noise sources and can be turned on unintentionally. The short-circuit current reaches harmful levels within hundreds of nanoseconds. Therefore, a short-circuit protection method based on sensing voltage across the layout inductance is applied on a parallel switch half-bridge. The implementation of a short-circuit protection technique on a parallel configuration is different from a single bridge configuration due to symmetric layout design constraints. Reported SC protection methods in the literature are evaluated and compared for parallel configuration. The proposed layout based SC protection method is advantageous for parallel configuration because the sense circuit does not have to be placed close to a transistor or a half-bridge which relaxes the space limitations and increases the flexibility for symmetric layout design.

Experimental results show that the short circuit protection mechanism is able to detect the fault in 40 ns. After detecting the fault, a soft turn-off process is initiated within 100 ns to keep transistors in the safe-operating-area. Short circuit fault is completely removed in 250 ns as a final step. Moreover, experimental results also show that the proposed method does not deteriorate the power loop or the gate loop layouts. As a result of optimized layout design, the gate voltage is not distorted by the miller capacitance which could have initiated a short-circuit fault easily.

The proposed board can be adapted to many applications with increased current capability by paralleling and with its short-circuit protection ability. In this thesis, designed half-bridge boards are used in a bi-directional DC/DC converter application

where 5.24 kW/l or 85.9 W/in^3 of power density is achieved under full load. In order to reduce the size of passive components, the switching frequency is increased up to 450 kHz. The switching losses are eliminated by zero voltage switching obtained by quasi-square wave zero voltage switching. The high ripple of the inductor is canceled by interleaving two half-bridges. As a result, a very dense converter design is reached where the 20 A at 270 V is available as output in the buck mode. Similarly, the converter is able to supply up to 5.4 kW with 400 V output voltage in the boost mode. The design is verified with thermal tests. The estimated junction temperature of GaN HEMT rises up to 137 °C where the temperature over passive components does not exceed 100 °C. Lastly, 97.7% efficiency and 98.7% efficiency are obtained under full load conditions for the buck mode and the boost mode, respectively.

Moreover, the proposed converter and the non-isolated DC/DC converters in the literature are compared in Fig. 6.1. The presented converters include bi-directional converters with and uni-directional buck or boost converters with soft-switching. The detailed specs of the converters are presented in Table 6.1. Si based MOSFET is the most common semiconductor used in these converters; however, SiC and GaN switches have an increasing trend in the last years. On the one hand, it is clearly seen

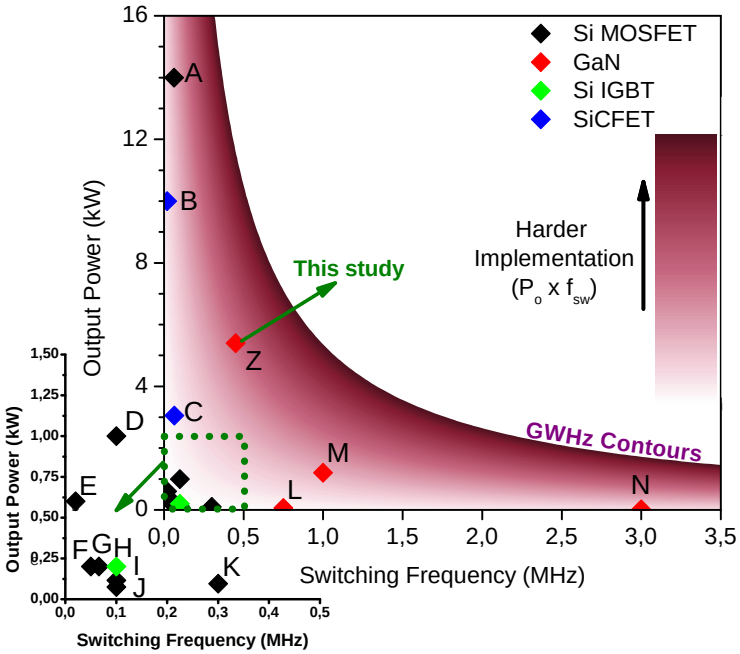


Figure 6.1: Comparison of DC/DC converters proposed in the literature

Table 6.1: Specs of the given converters on Fig. 6.1

	Study	P_o	f_{sw}	Topology	Device
A	Pavlovsky et al. [42]	14 kW	66 kHz	MBB*	Si MOSFET
B	Rodriguez et al. [67]	10 kW	20 kHz	Boost	SiCFET
C	Stevanovic et al. [68]	3.05 kW	64 kHz	Boost	SiCFET
D	Konjedic et al. [41]	1 kW	100 kHz	Buck & Boost	Si MOSFET
E	Sinha et al. [69]	600 W	20 kHz	Buck	Si MOSFET
F	Yang et al. [40]	200 W	50 kHz	MBB	Si MOSFET
G	Das et al. [38]	200 W	66 kHz	MBB	Si MOSFET
H	Ahmadi et al. [70]	200 W	100 kHz	MBB	Si IGBT
I	Chen et al. [44]	115 W	100 kHz	MBB	Si MOSFET
J	Veerachary [71]	75 W	100 kHz	Modified Buck	Si MOSFET
K	Mao et al. [43]	96 W	300 kHz	MBB	Si MOSFET
L	Pajnìc et al. [72]	60 W	750 kHz	MBB	GaN
M	Huang et al. [39]	1.2 kW	1 MHz	MBB	GaN
N	Lee et al. [73]	20 W	3 MHz	Buck	GaN
Z	This study	5.4 kW	450 kHz	Buck & Boost	GaN

(*) Modified Buck & Boost topology

that MOSFET or IGBT based converters do not go beyond a certain level of switching frequency. On the other hand, GaN switches are preferred for lower power applications in general. It is seen that SiCFETs take the place of Si MOSFETs in recent years, leading improvement in power density. Furthermore, in Fig. 6.1, color contours are plotted where the color gets darker for increasing output power and switching frequency multiplication. Converters evidently position closer to an axis which is either output power axis or switching frequency axis. This fact is due to implementation hardness of increasing output power and switching frequency at the same time. These two parameters are hardly increased together for a couple of reasons. Firstly, the device has certain limitations in terms of switching speed and conduction losses. The figure-of-merit of the device ($Q_g * R_{ds-on}$) is the limiting factor and apparently, this limit can only be exceeded by using a different device. Secondly, many off the

shelf passive components are not satisfactory for high power, high-frequency applications. For example, the inductors are not available for that region because increasing current requires longer air-gap or larger core volume. This results in higher winding or core losses on the inductor. Similarly, off-the-shelf capacitors cannot respond to the demands of increasing power and switching frequency at the same time. This is because of their internal resistance and frequency responses. Related to the second reason, another limit is cooling. The natural cooling or air cooling would not be enough to cool down both transistors and passive components for a high frequency, high power application. Liquid cooling is an option to exceed the limits but this is not a reasonable option unless a liquid reservoir is already available in the system. The proposed converter design utilizes the advantage of low on-state resistance of GaN HEMTs rather than increasing the switching frequency. Therefore, the proposed converter is closer to the power axis in Fig. 6.1.

6.2 Areas for Improvement

Due to GaN HEMTs being new in the industry, the following years will bring significant improvements in power electronics technology changing our daily life. It can be expected to have smaller and lighter charge units, electric vehicles with improved ranges, smaller photovoltaic inverters for home usage, and many different types of power converters. Therefore, it can be expected for GaN HEMTs to stay as a hot topic in academia for the following years as well. This study is a part of this journey by covering both characterization and application sides of GaN HEMTs. Nevertheless, there is a wide research space regarding this thesis' topic and GaN HEMTs in general:

1. **Characterization of device parameters:** The main intention behind GaN HEMTs' usage is to increase efficiency and power density. Therefore, the maximization of switching frequency should be aimed. However, increased switching frequency makes soft-switching compulsory. As a result, the following parameters should be evaluated with respect to the frequency and the switching method:

- **Input charge and capacitance** of the device are key elements defining device figure-of-merit. Low input capacitance is a must for high switching frequencies (>10 MHz). Even though the input capacitance is assumed to be irrelevant to switching frequency, the relation between input charge and frequency has to be investigated further. More importantly, the results highlight the differences in the gate charge between hard-switching (6.1 nC) and soft-switching (5.0 nC). Therefore, the effect of switching speed on the gate charge could be analyzed. The tight dead-time adjustment also requires accurate estimation of input capacitance.
- **Output capacitance** is the main reason for switching losses. Even though soft-switching topologies eliminate these losses, hard switching topologies are mainly preferred for the sake of easiness. The mechanism behind the output losses is now being studied by researchers and there is still more space for investigation of the relation between the output losses and frequency, voltage bias, switching topology, device paralleling, switching speed, etc..
- **Threshold level** which is very low for GaN HEMTs makes the GaN HEMTs susceptible to circuit noises. It is worth investigating how the threshold level is affected by junction temperature, the gate bias level, frequency, or the switching topology.
- **On-state resistance** of the GaN HEMTs is low in comparison to other devices. However, it increases with increasing temperature and the amount of the increase varies from device to device. Since the conduction losses and final operating temperature are directly related to on-state resistance, it has to be analyzed further. The dependence on temperature, voltage bias, and gate bias are among the important factors.

2. **Switching performance:** The understanding of switching behavior and performance of GaN HEMTs is critical since either it can maximize the performance or it can cause circuit failure. The fault mechanisms experienced during the switching period has to be studied and understood. The false turn-on mechanism and preventive solutions are very important to satisfy reliability requirements. The effects of temperature, voltage bias, frequency, gate resistances, and

feedback mechanisms can be studied. The problems regarding these parameters can be solved by different gate driver topologies. Moreover, the layout parameters, parasitic inductances, and capacitances, the packaging technologies can be studied to see their effects more clearly.

3. **Layout design:** The small package size of GaN HEMTs leads to a great shrink in converter sizes. Therefore, the space on the printed circuit board (PCB) has to be used wisely. Reducing the number of components is possible with the optimization of layout designs. For example, less number of power loop bypass capacitors can be used if the power loop inductance decreases. An interesting study topic would be the investigation of the effect of different PCB manufacturing techniques on the power loop and the gate loop. Further, gate driver topologies that do not require an isolated power supply can be an effective solution to have compact designs. Moreover, device paralleling is a challenging point especially for a large number of parallel transistors. The simultaneous switching of parallel-connected transistors is a must and it gets harder with the increasing number of transistors. Therefore, the gate loop design needs to be improved for an increased number of parallel-connected transistors. Lastly, monolithic GaN power transistors reduce the stress of layout design significantly, so high switching speeds could be achieved with this type of GaN switches.

4. **Reliability:** Since the manufacturing technologies of GaN HEMTs are not mature yet, a significant variation on the device parameters can be observed. The variation of the device parameters with respect to temperature, time, voltage bias or ambient conditions, etc. can be a comprehensive research topic in terms of device reliability.

    - **Thermal effects** can influence the operation vitally. Device losses, switching speed, etc. are related to the device temperature. Each device gets affected differently from temperature. The variation of the parameters with temperature has to be minimized by the manufacturer. Also, the designer should be aware of varying parameters with respect to temperature. Therefore, a characterization and reliability study can illuminate the nature of the device.

- **Voltage bias** changes the on-state resistance of the GaN HEMTs which is known as the current collapse phenomenon. An understanding of how much device resistance deviates under voltage can be tested. Moreover, it is worth studying the effect of the current collapse on stability. On top of increased conduction losses, the device's switching performance can be investigated by taking the current collapse into account.
- **Short circuit (SC)** ruggedness of GaN HEMTs is lower than other types of transistors. The mechanisms causing short circuit have to be identified clearly to inhibit the risk of SC. Moreover, fast and reliable protection methods are required. The protection method, proposed in this thesis, is effective against shoot-through type SC faults. Moreover, it is required to investigate the performances of different protection methods for parallel-connected devices. Also, it is worth to study how the protection methods give the result for multiple numbers of parallel-connected transistors. Further, the SC protection mechanism can be improved so that fault-underload could also be detected. An important improvement would be reducing the required space for SC protection. Instead of turning-off transistors with a digital signal processor (DSP), an analog implementation might reduce the cost by removing the requirement of a DSP with high clock speed.

5. **Topologies:** Various power converter topologies have been proposed and tested already in the literature. It is potentially a valuable research area to investigate how the classical topologies act with GaN HEMTs. It is important to see their efficiency performance, volume minimization, and cost considerations with GaN HEMTs. However, a more valuable study would be to reintroduce the previous topologies evaluated as less feasible with former semiconductor devices. Unfeasible converter topologies would be advantageous with GaN HEMT semiconductors.

    - **Passive components** are the limiting factors of today's power converters. The potential frequency and power range of GaN HEMTs are hardly assisted by the inductors and capacitors on the shelf. Design and manufacturing of magnetic cores, winding topologies, and wires get challenging if

the frequency and the power increase together. Different winding topologies with coupled or non coupled magnetic cores can be proposed. The quasi-square wave zero voltage switching Buck/Boost topology also can be improved significantly with a coupled inductor design. Moreover, the capacitors are limited as well for the high voltage range if the switching frequency is also high. Evaluation of the capacitors on the market is important before assigning operating conditions of any topology.

- **Multilevel topologies** draw huge attention for GaN-based applications. Since the maximum voltage is limited for GaN HEMTs, multilevel topologies might be a solution to reach higher voltage levels. Moreover, the rapid dV/dt change of GaN HEMTs is a concern for motor drive applications due to the isolation safety of motor winding. A multi-level inverter solution would be helpful to reduce dV/dt stress.
- **Cooling components** also plays a significant role in the power density of the converter. GaN HEMTs' small cooling surface area requires good contact with heat sinks. There are different types of thermal interface materials and heat sinks. Whichever thermal interface material is used, the heat sink has to be connected to the printed circuit board closely which reduces the space utilization on the PCB. A custom design heat sink solution would help to improve the compactness of the converters. Natural cooling is also a trend for increasing the long term reliability of converters. Therefore, topology selection and proper thermal design are critically important for power density and reliability.

In summary, there are many potential research fields regarding GaN HEMTs from the characterization of the device to end-product converters. Therefore, GaN HEMTs will be occupying power electronics in academia and industry for long years.

REFERENCES

[1] E. A. Jones, F. F. Wang, and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 707–719, 2016.

[2] A. Lidow, J. Strydom, M. de Rooij, and D. Reusch, *GaN Transistors for Efficient Power Conversion*. California, USA: Wiley, 2nd ed., 2015.

[3] M. Fernandez, X. Perpina, J. Roig-Guitart, M. Vellvehi, F. Bauwens, M. Tack, and X. Jorda, "Short-Circuit Study in Medium-Voltage GaN Cascodes, p-GaN HEMTs, and GaN MISHEMTs," *IEEE Transactions on Industrial Electronics*, vol. 64, pp. 9012–9022, nov 2017.

[4] GaN Systems, Ottawa, Canada, *GS66508T Top-side cooled 650 V E-mode GaN transistor Preliminary Datasheet*, 2020. Rev. 200402.

[5] GaN Systems, Ottawa, Canada, *GS66508B Bottom-side cooled 650 V E-mode GaN transistor Preliminary Datasheet*, 2019. Rev. 190502.

[6] R. Hou, J. Lu, and D. Chen, "An Ultrafast Discrete Short-Circuit Protection Circuit for GaN HEMTs," *2018 IEEE Energy Conversion Congress and Exposition, ECCE 2018*, pp. 1920–1925, 2018.

[7] M. Landel, S. Lefebvre, D. Labrousse, C. Gautier, F. Zaki, and Z. Khatir, "Dispersion of electrical characteristics and short-circuit robustness of 600V E-mode GaN transistors," *PCIM Europe 2017 - International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, no. May, pp. 16–18, 2017.

[8] F. Karakaya, M. Ugur, and O. Keysan, "Investigation of Turn-on and Turn-off Characteristics of Enhancement-Mode GaN Power Transistors," (Riga), pp. 1–10, EPE Association, 2018.

[9] R. Xie, H. Wang, G. Tang, X. Yang, and K. J. Chen, "An Analytical Model for False Turn-On Evaluation of High-Voltage Enhancement-Mode GaN Transistor in Bridge-Leg Configuration," *IEEE Transactions on Power Electronics*, vol. 32, no. 8, pp. 6416–6433, 2017.

[10] A. Jafari, M. S. Nikoo, F. Karakaya, and E. Matioli, "Enhanced DAB for Efficiency Preservation Using Adjustable-Tap High-Frequency Transformer," *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 6673–6677, 2020.

[11] M. J. Liu and S. S. Hsu, "A Miniature 300-MHz Resonant DC-DC Converter with GaN and CMOS Integrated in IPD Technology," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9656–9668, 2018.

[12] R. Xie, X. Yang, G. Xu, J. Wei, Y. Wang, H. Wang, M. Tian, F. Zhang, W. Chen, L. Wang, and K. J. Chen, "Switching Transient Analysis for Normally-Off GaN Transistors with p-GaN Gate in a Phase-Leg Circuit," *IEEE Transactions on Power Electronics*, vol. PP, no. c, pp. 1–1, 2018.

[13] A. Jafari, M. Samizadeh Nikoo, N. Perera, H. K. Yildirim, F. Karakaya, R. Soleiman Zadeh Ardebili, and E. Matioli, "Comparison of Wide-band-gap Technologies for Soft-Switching Losses at High Frequencies," *IEEE Transactions on Power Electronics*, vol. 8993, no. c, pp. 1–1, 2020.

[14] N. Perera, G. Kampitsis, R. Van Erp, J. Ancay, A. Jafari, M. S. Nikoo, and E. Matioli, "Analysis of Large-Signal Output Capacitance of Transistors using Sawyer–Tower Circuit," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6777, no. c, pp. 1–1, 2020.

[15] Z. Tong, G. Zulauf, J. Xu, J. D. Plummer, and J. Rivas-Davila, "Output Capacitance Loss Characterization of Silicon Carbide Schottky Diodes," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 865–878, 2019.

[16] M. Samizadeh Nikoo, A. Jafari, N. Perera, and E. Matioli, "Measurement of Large-Signal COSS and COSS Losses of Transistors Based on Nonlinear Resonance," *IEEE Transactions on Power Electronics*, vol. 35, no. 3, pp. 2242–2246, 2020.

[17] E. A. Jones, F. Wang, and B. Ozpineci, "Application-based review of GaN HFETs," *2nd IEEE Workshop on Wide Bandgap Power Devices and Applications, WiPDA 2014*, pp. 24–29, 2014.

[18] E. A. Jones, F. Wang, D. Costinett, Z. Zhang, B. Guo, B. Liu, and R. Ren, "Characterization of an enhancement-mode 650-V GaN HFET," *2015 IEEE Energy Conversion Congress and Exposition, ECCE 2015*, pp. 400–407, 2015.

[19] K. Peng, S. Eskandari, and E. Santi, "Characterization and Modeling of a Gallium Nitride Power HEMT," *IEEE Transactions on Industry Applications*, vol. 52, no. 6, pp. 4965–4975, 2016.

[20] K. Wang, X. Yang, H. Li, H. Ma, X. Zeng, and W. Chen, "An Analytical Switching Process Model of Low-Voltage eGaN HEMTs for Loss Calculation," *IEEE Transactions on Power Electronics*, vol. 31, pp. 635–647, jan 2016.

[21] G. Wang, J. Mookken, J. Rice, and M. Schupbach, "Dynamic and static behavior of packaged silicon carbide MOSFETs in paralleled applications," *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, pp. 1478–1483, 2014.

[22] J. Lu, R. Hou, and D. Chen, "Loss Distribution among Paralleled GaN HEMTs," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 1914–1919, IEEE, sep 2018.

[23] J. Lu and D. Chen, "Paralleling GaN E-HEMTs in 10kW-100kW systems," *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, pp. 3049–3056, 2017.

[24] N. Haryani, J. Wang, and R. Burgos, "Paralleling 650 V/ 60 A GaN HEMTs for high power high efficiency applications," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, vol. 3, (Cincinnati, OH, USA), pp. 3663–3668, IEEE, oct 2017.

[25] N. Sang, P.-O. Jeannin, and P. Lefranc, "Analyses of the unbalanced paralleled GaN HEMT transistors," *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, pp. 1–9.

[26] N. Badawi, A. E. Awwad, and S. Dieckerhoff, "Robustness in short-circuit mode: Benchmarking of 600V GaN HEMTs with power Si and SiC MOSFETs," *ECCE 2016 - IEEE Energy Conversion Congress and Exposition, Proceedings*, pp. 1–7, 2016.

[27] B. Huang, Y. Li, T. Q. Zheng, and Y. Zhang, "Design of overcurrent protection circuit for GaN HEMT," in *2014 IEEE Energy Conversion Congress and Exposition, ECCE 2014*, pp. 2844–2848, 2014.

[28] X. Lyu, S. Bala, H. Li, Y. Abdullah, K. Wang, B. Hu, Z. Yang, J. Liu, J. Wang, and L. Liu, "A Reliable Ultra-Fast Short Circuit Protection Method for E-mode GaN HEMT," *IEEE Transactions on Power Electronics*, vol. 8993, no. c, pp. 1–1, 2020.

[29] J. Acuna, J. Walter, I. Kallfass, and G. N. Gan, "Very Fast Short Circuit Protection for Gallium-Nitride Power Transistors Based on Printed Circuit Board Integrated Current Sensor Keywords," in *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, (Riga), pp. 1–10, 2018.

[30] K. Sun, J. Wang, R. Burgos, D. Boroyevich, Y. Kang, and E. Choi, "Analysis and design of an overcurrent protection scheme based on parasitic inductance of SiC MOSFET power module," *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, vol. 2018-March, pp. 2806–2812, 2018.

[31] E. A. Jones, P. Williford, and F. Wang, "A fast overcurrent protection scheme for GaN GITs," *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications, WiPDA 2017*, vol. 2017-Decem, pp. 277–284, 2017.

[32] K. Wang, Y. M. Abdullah, X. Li, D. Xing, J. Wang, L. Liu, and S. Bala, "A Reliable Short-Circuit Protection Method with Ultra-Fast Detection for GaN based Gate Injection Transistors," in *2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, vol. 0, pp. 43–46, IEEE, oct 2019.

[33] R. Hou and J. Lu, "An ultrafast discrete protection circuit utilizing multi-

functional dual-gate pads of GaN HEMTs," *2019 IEEE Energy Conversion Congress and Exposition, ECCE 2019*, pp. 818–823, 2019.

[34] A. E. Awwad and S. Dieckerhoff, "Short-circuit evaluation and overcurrent protection for SiC power MOSFETs," *2015 17th European Conference on Power Electronics and Applications, EPE-ECCE Europe 2015*, 2015.

[35] O. S. Alemdar, F. Karakaya, and O. Keysan, "PCB layout based short-circuit protection scheme for GaN HEMTs," *2019 IEEE Energy Conversion Congress and Exposition, ECCE 2019*, pp. 2212–2218, 2019.

[36] S. Musumeci, R. Pagano, A. Raciti, F. Frisina, and M. Melito, "Parallel strings of IGBTs in short circuit transients: Analysis of the parameter influence and experimental behavior," *IECON Proceedings (Industrial Electronics Conference)*, vol. 1, pp. 555–560, 2002.

[37] C. Timms, L. Qiao, F. Wang, Z. Zhang, and D. Dong, "Oscillatory False Triggering of Parallel Si and SiC MOSFETs during Short-Circuit Tum-off," *2018 IEEE Energy Conversion Congress and Exposition, ECCE 2018*, pp. 383–386, 2018.

[38] P. Das, S. A. Mousavi, and G. Moschopoulos, "Analysis and design of a nonisolated bidirectional ZVS-PWM DC-DC converter with coupled inductors," *IEEE Transactions on Power Electronics*, vol. 25, no. 10, pp. 2630–2641, 2010.

[39] X. Huang, F. C. Lee, Q. Li, and W. Du, "High-Frequency High-Efficiency GaN-Based Interleaved CRM Bidirectional Buck/Boost Converter with Inverse Coupled Inductor," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4343–4352, 2016.

[40] J. W. Yang and H. L. Do, "High-efficiency bidirectional dc-dc converter with low circulating current and ZVS characteristic throughout a full range of loads," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3248–3256, 2014.

[41] T. Konjedic, L. Korošec, M. Truntič, C. Restrepo, M. Rodič, and M. Milanovič, "DCM-based zero-voltage switching control of a bidirectional DC-DC converter

with variable switching frequency," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 3273–3288, 2016.

[42] M. Pavlovsky, G. Guidi, and A. Kawamura, "Buck/boost DC-DC converter topology with soft switching in the whole operating region," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 851–862, 2014.

[43] H. Mao, O. Abdel Rahman, and I. Batarseh, "Zero-voltage-switching DC-DC converters with synchronous rectifiers," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 369–378, 2008.

[44] G. Chen, L. Chen, Y. Tao, Y. Deng, and X. He, "Zero-voltage-switching synchronous buck converter with coupled inductor," *Diangong Jishu Xuebao/Transactions of China Electrotechnical Society*, vol. 31, no. 8, pp. 102–110, 2016.

[45] W. Lee, D. Han, C. Morris, and B. Sarlioglu, "Minimizing switching losses in high switching frequency GaN-based synchronous buck converter with zero-voltage resonant-transition switching," *9th International Conference on Power Electronics - ECCE Asia: "Green World with Power Electronics", ICPE 2015-ECCE Asia*, pp. 233–239, 2015.

[46] Q. Huang and A. Q. Huang, "Variable Frequency Average Current Mode Control for ZVS Symmetrical Dual-Buck H-Bridge All-GaN Inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. PP, no. c, pp. 1–1, 2019.

[47] Texas Instruments, Texas, USA, *LMG1020 5-V, 7-A, 5-A Low-Side GaN and MOSFET Driver For 1-ns Pulse Width Applications*, 2018. Rev. B.

[48] Würth Elektronik, Germany, *WE-HCF Round Wire SMT High Current Inductor 74437529203151*, 2020.

[49] K. Wang, X. Yang, L. Wang, and P. Jain, "Instability Analysis and Oscillation Suppression of Enhancement-Mode GaN Devices in Half-Bridge Circuits," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1585–1596, 2018.

[50] GaN Systems, Ottawa, Canada, *GN009 Application Note: PCB Layout Considerations with GaN E-HEMTs*, 2019.

[51] X. Huang, Q. Li, Z. Liu, and F. C. Lee, "Analytical loss model of high voltage GaN HEMT in cascode configuration," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2208–2219, 2014.

[52] GaN Systems, Ottawa, Canada, *SPICE model for GaN HEMT - usage guidelines and example*, 2016. Rev. 9.

[53] GaN Systems, Ottawa, Canada, *GS66508T/GS66516T-EVBDB GaN EHEMT Daughter Board and GS665MB-EVB Evaluation Platform User's Guide*, 2018. Rev. 180126.

[54] K. Wang, X. Yang, H. Li, L. Wang, and P. Jain, "A High-Bandwidth Integrated Current Measurement for Detecting Switching Current of Fast GaN Devices," *IEEE Transactions on Power Electronics*, vol. 33, pp. 6199–6210, jul 2018.

[55] Laird Technologies, Missouri, USA, *Tpli 200 Series Thermal Gap Filler*, 2018.

[56] CTS, Illionis, USA, *Forged Heat Sinks with Plate Fins*, 2018.

[57] Orion Fans, Texas, USA, *OD3510 Series*, 2019.

[58] FLIR, Portland, USA, *FLIR E4, E5, E6, E8 with MSX® Enhancement*, 2013. Rev. 09/13.

[59] M. A. Khan, A. Ahmed, I. Husain, Y. Sozer, and M. Badawy, "Performance Analysis of Bidirectional DC-DC Converters for Electric Vehicles," *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3442–3452, 2015.

[60] Y. S. Lee and G. T. Cheng, "Quasi-resonant zero-current-switching bidirectional converter for battery equalization applications," *IEEE Transactions on Power Electronics*, vol. 21, no. 5, pp. 1213–1224, 2006.

[61] M. März, A. Schletz, B. Eckardt, S. Egelkraut, and H. Rauh, "Power electronics system integration for electric and hybrid vehicles," *2010 6th International Conference on Integrated Power Electronics Systems, CIPS 2010*, pp. 16–18, 2011.

[62] FerroxCube, Taiwan, *E32/6/20/R Planar E cores and accessories*, 2008. Rev. 01-Sep-2008.

[63] FerroxCube, Taiwan, *E38/8/25 Planar E cores and accessories*, 2008. Rev. 01-Sep-2008.

[64] KEMET, Florida, USA, *Surface Mount Polyethylene Naphthalate (PEN) Film Capacitor LDE, Unencapsulated Stacked Chip, Size 1206 – 6054, 50 – 1,000 VDC (Automotive Grade)*, 2020. Rev. 20-Apr-2020.

[65] Vishay, Pennsylvania, USA, *AC and Pulse Double Metallized Polypropylene Film Capacitors MMKP Radial Potted Type*, 2018. Rev. 08-Aug-2018.

[66] A. Jafari, M. Heijnemans, R. Soleiman Zadeh Ardebili, R. van Erp, M. Samizadeh Nikoo, E. Figini, F. Karakaya, and E. Matioli, "High-Accuracy Calibration-Free Calorimeter for the Measurement of Low Power Losses," *IEEE Transactions on Power Electronics*, vol. 8993, no. 1, pp. 1–1, 2020.

[67] A. Rodriguez, A. Vazquez, M. R. Rogina, and F. Briz, "Synchronous Boost Converter With High Efficiency at Light Load Using QSW-ZVS and SiC mosfets," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 386–393, 2018.

[68] B. Stevanovic, D. Serrano, M. Vasic, P. Alou, J. A. Oliver, and J. A. Cobos, "Highly Efficient, Full ZVS, Hybrid, Multilevel DC/DC Topology for Two-Stage Grid-Connected 1500-V PV System with Employed 900-V SiC Devices," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 811–832, 2019.

[69] M. Sinha, J. Poon, B. B. Johnson, M. Rodriguez, and S. V. Dhople, "Decentralized Interleaving of Parallel-connected Buck Converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4993–5006, 2019.

[70] M. Ahmadi, M. Mohammadi, E. Adib, and H. Farzanehfard, "Family of non-isolated zero current transition bi-directional converters with one auxiliary switch," *IET Power Electronics*, vol. 5, no. 2, p. 158, 2012.

[71] M. Veerachary, "Analysis of minimum-phase fourth-order buck DC-DC converter," *IEEE Transactions on Industrial Electronics*, vol. 63, pp. 144–154, jan 2016.

[72] M. Pajnić and P. Pejović, “Zero-Voltage Switching Control of an Interleaved Bi-Directional Buck-Boost Converter with Variable Coupled Inductor,” *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9562–9572, 2019.

[73] W. Lee, D. Han, C. Morris, and B. Sarlioglu, “Minimizing switching losses in high switching frequency GaN-based synchronous buck converter with zero-voltage resonant-transition switching,” *9th International Conference on Power Electronics - ECCE Asia: "Green World with Power Electronics", ICPE 2015-ECCE Asia*, pp. 233–239, 2015.

APPENDIX A

SUPPLEMENTARY DOCUMENTS

All documents supposed to be placed in this chapter are shared on the following link:

https://github.com/furkankarakaya/GaN-Studies/tree/master/Thesis/Appendix

The following documents can be found on that webpage:

- Personal background
- Academic papers
- Simulation files for Chapter 3
- Simulation files of Buck and Boost converters
- PCB view and documents for:
    1. Gate charge characterization board
    2. Output capacitance characterization board
    3. Control board
    4. Converter board
    5. Half-bridge board

Figure A.1: You can access the appendix documents via this QR code